D O M A I N

Order No. 008778
Revision 03

Domain Series 3000/Series 4000 Technical Reference

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FCC REGULATIONS

The Federal Communications Commission (FCC) of the U.S. government regulates the radio frequency energy emanated by computing devices through published regulations. These regulations specify the limits of radio frequency emission to protect radio and television reception. All Domain nodes and peripherals have been tested and comply with these limits. The FCC regulations also require that computing devices used in the U.S. display the agency's label and that the related documentation include the following statement.

WARNING: This equipment generates, uses, and may emit radio frequency energy and, if not installed and used in accordance with these instructions, may cause interference to radio communications. It has been tested and found to comply with the limits for a Class A computing device pursuant to Subpart J of Part 15 of FCC Rules, which are designed to provide reasonable protection against such interference when operated in a commercial environment. Operation of this equipment in a residential area is likely to cause interference, in which case the user at his own expense will be required to take whatever measures may be required to correct the interference.

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Preface

This manual contains interface connection and performance specification information for the Domain® Series 3000™ and Series 4000™ Personal Workstations™. This manual is intended for Series 3000 or 4000 System Builders who require specific interface information for this equipment. Consult the *Domain Series 3000/Series 4000 Hardware Architecture Handbook* for additional information.

The Domain System can include a Disk/Floppy or a Disk/Tape storage option configuration. Although your system may not be equipped with these options, all possible devices are described in this manual. Use only the material that pertains to your particular configuration.

This manual contains 16 chapters and one appendix arranged as follows:

Chapter 1 provides an overview of the Series 3000/Series 4000 systems, including functional descriptions of major subassemblies.

Chapter 2 describes the AT-compatible bus operation and interface requirements.

Chapter 3 describes the CPU/Motherboard operation and interface requirements.

Chapter 4 describes the power supply operation and power requirements.

Chapter 5 describes the Winchester/floppy disk controller operation and interface requirements.

Chapter 6 describes the Winchester disk drive operation and interface requirements.

Chapter 7 describes the floppy disk drive operation and interface requirements.

Chapter 8 describes the tape cartridge controller operation and interface requirements.

Chapter 9 describes the tape cartridge drive operation and interface requirements.

Chapter 10 describes the graphics controllers operation and interface requirements.

Chapter 11 describes the monitors operation and interface requirements.

Chapter 12 describes the Domain low-profile keyboard operation and interface requirements.

Chapter 13 describes the mouse pointing device operation and interface requirements.

Chapter 14 describes the 802.3 network controller board operation and interface requirements.

Chapter 15 describes the serial/parallel controller board operation and interface requirements.

Chapter 16 describes the PC coprocessor board operation and interface requirements.

Appendix A contains timing diagrams for bus operations.

Related Manuals

For further information on the Series 3000 and Series 4000 systems, refer to *Unpacking and Installing Your DN3000/DN4000 Personal Workstation and the DSP3000/DSP4000 Server* (007857), *Operating the DN3000/DN4000 Personal Workstation and DSP3000/DSP4000 Server* (007858), and *Servicing the Domain Series 3000/Series 4000* (007859).

For Series 3000 and Series 4000 system architecture information, see the *Domain Series 3000/Series 4000 Hardware Architecture Handbook* (007861). For information about using the system, see the manuals *Getting Started with Your Domain System* (002348) and the *Domain System Command Reference* (002547).

For information about installing network software, creating and maintaining the Domain Network Registry, and troubleshooting network problems, see *Administering Your Domain System* (001746).

For Domain system diagnostic information, see *Using Domain Diagnostics* (009329).

For information about installing peripherals supported by Domain software, see *Installing Input/Output (I/O) Devices for Domain Nodes* (008268), *Writing Device Drivers with GPIO Calls* (000959), and *Installing and Programming the Domain Series 3000 SPE Option* (009798).

Naming Conventions

This document supports the Domain Series 3000 (DS3000) and Series 4000 (DS4000) systems. Where manual contents apply to both models, the words *Domain System* are used. Where contents apply to a specific model, the appropriate model name appears.

Problems, Questions, and Suggestions

We appreciate comments from the people who use our system. In order to make it easy for you to communicate with us, we provide the Reader's Response form at the back of this manual for documentation comments.

Electrostatic Discharge (ESD) Precautions

When installing a Printed Circuit Board (PCB), observe the following precautions to prevent electrostatic damage to Integrated Circuits (ICs).

- Stand on a static-free mat.
- Wear a ground strap to ensure that any accumulated electrostatic charge will be discharged from your body to ground.
- Ground all equipment together, including the static free mat, ground strap, routing nodes, and peripheral units.
- Keep uninstalled PCBs in their protective antistatic bags.
- Handle PCBs by their edges, once you have removed them from their antistatic bags.

FCC Compliance

Any third party I/O device installed in the DS3000 or DS4000 must be FCC compliant in accordance with the requirements set forth on the title page of this manual. In the event that a third-party noncompliant I/O device is installed, the customer assumes all responsibility and liability arising therefrom.

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Chapter 1

Theory of Operation

This chapter describes the theory of operation for the Domain Series 3000 and Series 4000 workstations. The purpose of this chapter is to give you an understanding of the basic system operation to the subassembly level.

1.1 System-Level Operation

The DS3000 and DS4000 systems are compatible with both the Domain network and the operating system, as well as with AT bus-compatible devices. To achieve this goal, the *Domain Systems* use a dual bus architecture that combines a system bus with the AT-compatible bus through the AT bus-compatible interface. By using this dual bus architecture, the *Domain System* has the speed and power of the 32-bit MC68020, along with the flexibility to run AT-compatible devices.

This section presents a general overview of the operating system, and discusses several topics that apply to the system as a whole, rather than to individual subassemblies. Refer to Section 1.5 for more details about individual subassemblies.

1.2 System Buses and the Bus Interface

Figures 1-1 and 1-2 show the functional organization of the buses and bus interface on the DS3000 and DS4000 CPU/Motherboards. The system bus provides the main channel for address and data flow between the CPU, FPU, MMU and main memory. The AT-compatible bus supports the various device controllers, system devices, and other options. The bus interface incorporates the DMA controller and Interrupt controller (described in the following sections), and the logic that converts the data and address format of the AT-compatible bus to the data and address format of the system bus (and back again).

Series 4000 Address Translation Map

The Series 4000, unlike the Series 3000, incorporates an address translation map in its architecture. The address translation map allows the Series 4000 to perform DMA to or from noncontiguous physical memory. The map also provides a 512-KB window through which external AT-compatible bus masters can access CPU main memory.

The address translation map contains one entry for each main memory page accessed via DMA controller or other external AT-compatible bus master. The operating system allocates a map entry each time DMA is requested. The map provides the interface between DMA controller address space and Series 4000 physical address space.

1.3 Virtual Bus

The MC68020 microprocessor generates a 32-bit virtual address accompanied by a 3-bit function code. In the Series 3000, the virtual address appears to "wrap" at 26 bits, the five high-order (27:31) bits are simply ignored. The Series 4000 makes use of all virtual address bits. Once gated onto the virtual bus, each address can be translated within, or passed directly through, the system memory management unit, or transferred to the floating-point coprocessor, or transferred to the interrupt vector-generation circuitry.

In the Series 4000, the virtual address can also be transferred to or from virtual cache. Once transferred to the virtual cache, address and data are transferred to the write buffer, which writes the data to physical memory. Refer to Subsections 1.3.1 and 1.3.2 for details on the virtual cache and write buffer.

1.3.1 Virtual Cache

The virtual cache is implemented in the Series 4000. It is an 8-KB, direct-mapped cache that contains 2048 4-byte instruction and/or data entries. The virtual cache uses a write-through with write-allocate design that causes the cache to be updated (along with main memory) for every memory write placed in the cache.

1.3.2 Write Buffer

The write buffer is a Series 4000 device (see Figure 1-2) that resides on the virtual bus between the microprocessor and the PMMU. This buffer allows the CPU to concurrently update the cache and execute cache read cycles without waiting for write cycles to complete.

1.4 System Interrupts

All of the devices shown on the AT-compatible bus in Figures 1-1 and 1-2 (except for the floppy drive) use interrupts to gain access to the CPU and memory. When the Interrupt controller receives an interrupt over one of the Interrupt Request (IRQ) lines on the AT-compatible bus (IRQ0 - IRQ15), the controller signals the CPU that one of the system devices requires attention. On the next available CPU cycle, the CPU performs an interrupt service routine appropriate for the device. The CPU then resumes normal operation until it receives another interrupt.

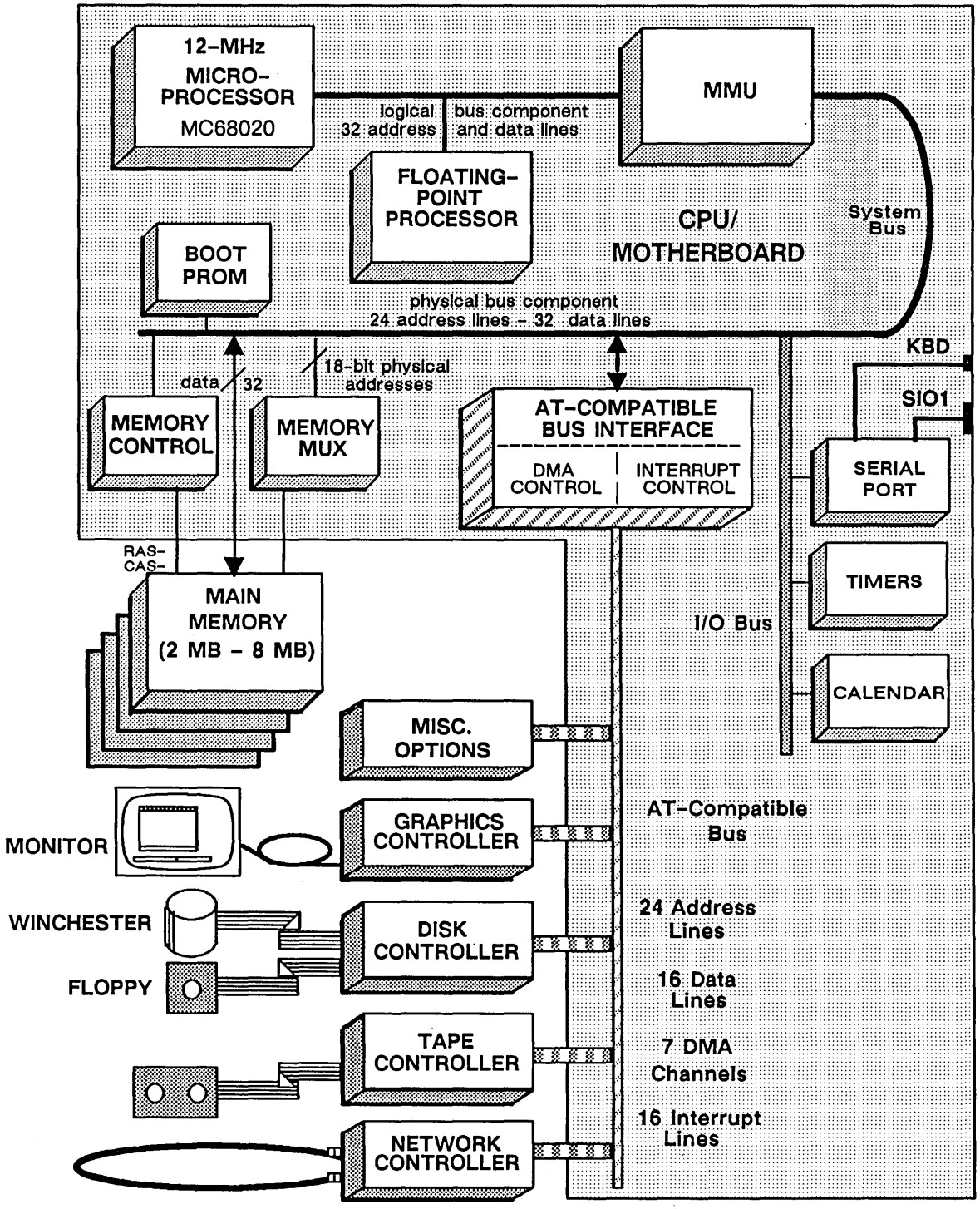

Figure 1–1. DS3000 Functional Block Diagram

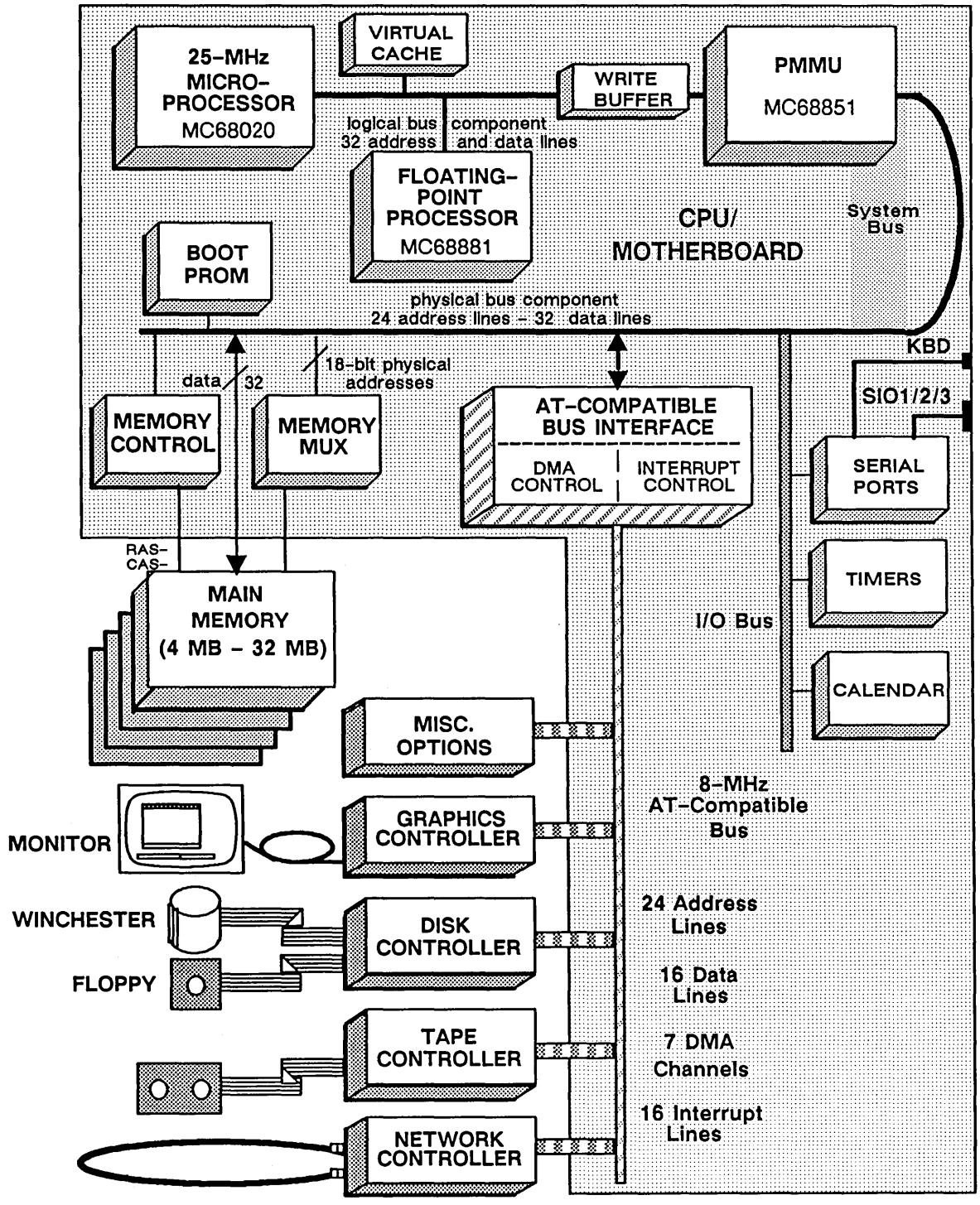

Figure 1-2. DS4000 Functional Block Diagram

1.5 Subassembly–Level Operation

This section describes the operation of the major subassemblies in the DS3000/DS4000 system. Refer to Figures 1–1 and 1–2 as you read the descriptions of these subassemblies.

1.5.1 CPU/Motherboard

The CPU/Motherboard controls the program flow in the system, and is the host for the memory module(s), device controllers, and other optional boards. The most important elements of the CPU/Motherboard's hardware are

- The MC68020 microprocessor, the system's CPU (DS4000 CPU operates at 25 MHz.)
- The MC68881 floating-point coprocessor (DS4000 FPU operates at 25 MHz)
- The DMA controller
- The interrupt controller
- The boot PROM
- The system timer
- The system clock and calendar with battery backup
- One full–duplex, programmable port for serial I/O. Three full–duplex, programmable ports for serial I/O in the DS4000.
- One full–duplex, programmable serial port for the keyboard
- Six PCB connectors compatible with PC/AT–type boards (seven AT–compatible slots on newer DS3000 systems and the DS4000)
- Two PCB connectors compatible with PC/XT–type boards (one XT–compatible slot on newer DS3000 systems and the DS4000)
- Four PCB connectors for the memory modules
- The system status LEDs

CPU and MMU/PMMU

The CPU executes MC68020 instructions in response to the operating system and user programs. The DS3000 MMU and DS4000 PMMU (MC68851) are coprocessing devices that perform iterative memory management routines which would otherwise use up valuable CPU processing time. The MMU/PMMU tracks main memory free space, performs logical–to–physical address translations, and swaps pages in and out of memory in response to the needs of the CPU (and DMA controller). The MMU/PMMU performs the following functions:

- When enabled, the MMU/PMMU associates every physical address with a virtual address; this association is called mapping, and the system operates in mapped mode as soon as the MMU/PMMU is operational.
- During online operation, the MMU/PMMU translates the virtual addresses of the pages into the physical addresses of the free space in main memory. Because of this translation, the mapping scheme for many locations in main memory changes constantly as the MMU/PMMU reassigns pages to different physical addresses in main memory. (The MMU/PMMU's original mapping scheme stays the same for pages that stay in main memory all the time and for locations not in main memory.)

As part of the interaction between the CPU and MMU/PMMU, the CPU passes virtual addresses from the operating system to the MMU/PMMU. (These addresses represent pages of memory needed by various processes.) When the MMU receives the virtual address of a page *currently in main memory,* an MMU/PMMU hit occurs because the page is already where it is needed. When the MMU/PMMU receives a virtual address *not currently in memory,* an MMU/PMMU miss occurs.

An MMU/PMMU miss generates a page fault condition, and the operating system responds by authorizing disk or network I/O to move the required page into memory. If there is not enough room in main memory, the operating system authorizes disk or network I/O to move an inactive page out of main memory.

FPU

The MC68881 floating-point coprocessor executes floating-point math routines in the hardware under the control of microcode. The FPU shares the CPU's access to the MMU/PMMU and memory. The FPU is not an active bus master because it never accesses memory directly. The MC68020 CPU fetches all operands for the FPU.

DMA Controller

The DMA controller contains logic for receiving requests from DMA devices (the floppy disk is the only DMA device), for querying whether a CPU transfer is enabled, and for opening a DMA channel. The AT-compatible bus has seven channels for DMA transfers, along with associated request and acknowledge lines (see Figure 1-1).

Channels 0 through 3 support 8-bit transfers to or from 8-bit devices. Channel 4 controls the cascade of channels 0 through 3 to the CPU. Channels 5 through 7 support 16-bit transfers to or from 16-bit devices.

Interrupt Controller

The Interrupt controller provides 16 system interrupt levels for the DS3000. All of the devices on the AT-compatible bus, with the exception of the floppy disk, use interrupts to request service by the CPU.

Boot PROM

The boot PROM stores a read-only copy of the Mnemonic Debugger (MD) program, and can perform diagnostics that check the fundamental operation of CPU board hardware.

Timers and the System Clock

In the DS3000, the system timers provide 4-, 8-, and 16-microsecond clock signals used by the operating system to schedule processes and time various operations. In the DS4000, system clocking is derived from a 25-MHz oscillator. The operating system uses the system clock (in conjunction with the system-ID RAM on the CPU/Motherboard) to provide the proper identification (hour and second) for object-creation operations such as file creation.

Calendar

The operating system uses the calendar (in conjunction with the system-ID RAM on the CPU/Motherboard) to provide the proper identification (day, month, and year) for object-creation operations such as file creation. Problems with object creation can indicate a failure in the calendar device or the calendar battery, or (less frequently), a failure in reading the system-ID RAM.

Serial Lines

In the DS3000, the serial I/O control component drives two asynchronous serial lines, SIO0 and SIO1; in the DS4000, four asynchronous lines are driven, SIO0, SIO1, SIO2, and SIO3. SIO0 is the dedicated serial line for the keyboard. SIO1, 2, and 3 are RS-232, general-purpose lines. All lines are fully programmable and support full-duplex communications.

External Connectors on the CPU/Motherboard

The AT/XT-compatible bus has eight connectors to accommodate the various system controllers and other options. All eight slots have a 62-pin connector for PC/XT-type PCBs. Six slots also have a 36-pin connector, which allows them to accept PC/AT-type PCBs. Newer DS3000 systems and the DS4000 have seven AT-compatible slots and one XT-compatible slot.

The system bus has four 70-pin connectors for the memory modules.

The SIO lines have a 9-pin DIN connector for the keyboard and a 25-pin, D-shell connector for the general-purpose lines. In the DS4000, a 3-port cable provides access to the three serial lines at the D-shell connector.

System Status LEDs
The nine LEDs (five on the front panel of the cabinet, and four inside on the CPU board) indicate the progress of the boot PROM through its initialization, and report status codes during normal operation and in the event of an error. Chapter 3 contains a description of the LEDs.

1.5.2 Memory Module

Early DS3000 systems use a 1-MB memory module. The system can accommodate a maximum of 4 MB (four 1-MB memory boards). The system's byte-parity checking logic can detect 1-bit memory errors. It displays the code *Uncorrectable Memory Error Detected* if an error occurs.

Memory for the first two memory modules ranges from physical address $1FFFFF to $2FFFFF. It ranges to a maximum of $4FFFFF with four modules in place.

Later DS3000 memory boards contain 2 MB of RAM. The system can accommodate a maximum of 8 MB (four boards). DS4000 memory boards contain either 4 or 8 MB of memory, providing up to 32 MB of memory. The system's byte-parity checking logic can detect 1-bit memory errors. It displays the code *Uncorrectable Memory Error Detected* if an error occurs.

Memory for the first module in the DS3000 ranges from physical address $1FFFFF to $2FFFFF. It ranges to a maximum of $8FFFFF with four modules in place. In the DS4000, memory ranges from physical address $1000000 to $17FFFFF with one 8-MB module; $1FFFFFF for two modules; $27FFFFF with three modules; and an upper address limit of $2FFFFFF with four 8-MB modules in place.

1.5.3 Display Controllers

The 4-plane color monitor controller produces a 60-Hz, noninterlaced graphics display on a high-resolution (1024 x 800 pixels) color monitor. The DN3000 4-plane color monitor controller incorporates:

- 512 KB of image memory arranged in four 128-KB planes
- A memory data path that provides registers, multiplexers, and logic support for bit-block transfers (BLTs) from the image memory to the display
- Video output logic that drives the monitor with video signals representing the image in the bit map
- A sync generator for the timing signals necessary to create the video output signals
- An interface for communications with the CPU via the AT-compatible bus
- Control logic that regulates the operation of the other functional units

The DN4000 color controller provides the same functions as those just listed, but the display buffer has eight memory planes, each consists of a 1024 pixel by 1024 line memory, with a resolution of 1024 pixels x 800 lines. The 8-plane controller also provides the following additional features.

- 256 simultaneous colors selectable from a palette of 16.7 million shades
- Flicker-free, 60-Hz, noninterlaced screen refresh
- Low cost, small physical size, and low power requirements
- Dual port 1-MB image memory using 64K x 4 DRAMs
- High-speed image and main memory BLTs facilitated by specialized gate arrays

The DN3000 high-resolution monochrome display controller has the following features:

- High-resolution 1280 x 1024 display
- Flicker-free, 60-Hz, noninterlaced screen refresh
- Low power requirements
- 256-KB image memory using high-density, dynamic, Dual-Ported Video RAMs
- High-speed image and main memory BLTs facilitated by a specialized gate array

The image memory stores a bit map of the images that the controller displays on the monitor. To display the images, the controller scans the bit map and sends the image to the monitor in a serial bit stream via a coax cable.

The AT-compatible bus is not involved in controller-to-monitor transfers; the display controller uses the bus only when it is reading from or writing to main memory via the CPU.

The DN4000 monochrome display controller provides all the preceding features at an 8-MHz clock speed to accomodate the higher speed DS4000 AT bus.

1.5.4 Network Controller

The network controller manages the system's interface to the ring network. In older DS3000s, a two-board set makes up the network controller. In newer DS3000s and the DS4000, a single-board controller provides the same functionality. These controllers incorporate:

- A modem for modulation and demodulation of data from the ring
- Input-filtering and amplification hardware that converts data from the ring to a digital bit stream
- Receive logic that converts digital data in serial format into parallel format
- Transmit logic that converts digital data in parallel format into serial format
- A dual-ported RAM buffer
- Control logic that regulates the operation of the other functional units
- Relays that remove the system from the ring during power-off or offline operation

To encode data for transfer to other systems, the Apollo Token Ring network uses a baseband modulation technique with a biphase signal that contains both clock and data information. For a system to **transmit** on the network, the network controller's transmit logic takes parallel-format data from the AT-compatible bus and serializes it. The modem then adds clock signals to the serial bit stream, creating the biphase signal.

For a system to **receive** data from the network, the modem separates the clock signals from the data bits. Other hardware corrects and stabilizes the clock data. The receive logic then converts the serial data into parallel format so that it can be sent to the bus interface logic and out over the AT-compatible bus in a transfer to memory.

The transmit logic also supplies control information that travels with the data; the receive logic decodes this control information in data received from the network.

Refer to *Administering Your Domain System* for information about the network. See the Preface for a complete list of related manuals and order numbers.

1.5.5 Storage Device Controllers

All DS3000 and DS4000 systems equipped with optional storage devices contain controllers to manage the Winchester disk drives and floppy disk or tape cartridge drives, and the interface to the DMA controller and the interrupt controller. The Winchester and floppy disk drives share the same controller board. The tape cartridge drive uses a separate controller board. The controller boards incorporate:

- Control logic for the Winchester disk (read, write, format, seek, etc.)
- Control logic for the floppy disk drive
- Control logic for the tape cartridge drive (located on a separate tape cartridge controller)
- Interface logic for requesting a DMA channel for the tape cartridge drive
- Interface logic for requesting a DMA channel for the floppy drive
- Interface logic for requesting an interrupt for the Winchester drive

Although the floppy disk controller and the Winchester disk controller share the same PCB, the design separates the control logic into two independent units, allowing full concurrent operations between the drives and the rest of the system. That is, the floppy controller could be handling a DMA transfer to the floppy at the same time the Winchester is making a programmed I/O data (interrupt) transfer to the system. The tape cartridge drive uses a totally separate controller board to manage its functions.

Chapter 2

AT-Compatible Bus

2.1 Overview

The AT-compatible bus provides a communications medium for processor, memory, and I/O resources over a parallel set of address, data, and control lines. It supports multiple bus mastership so that coprocessors can control the bus and normal DMA-to-memory cycles. It provides multiple interrupt levels to allow devices to transfer program control to the appropriate interrupt service routines.

The AT-compatible bus is backward compatible to the IBM PC/XT* (the IBM PC/AT* 8-bit predecessor). The DS3000 and DS4000 buses are compatible with both 8-bit and 16-bit devices.

The IBM PC/XT uses a 62-pin PCB edge connector to support 8-bit data transfers, a memory address space determined by 20 address lines (1 MB), memory and I/O data transfer cycle types, Direct Memory Access capability (DMA), and interrupts. One slot in the DS3000 and DS4000 supports this capability.

The IBM PC/AT adds a 36-pin PCB edge connector to the remaining board slots on the bus. This connector provides the additional eight data lines for 16-bit transfers, additional address lines (unlatched and with different timing characteristics) to support a 16-MB memory address space, more interrupts, more DMA channels (which support 16-bit data transfers), and the capability for an I/O adapter to obtain bus mastership.

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The AT-compatible bus supports:

- Seven board slots that are IBM PC/AT bus compatible
- One board slot that is IBM PC/XT bus compatible
- 64-KB I/O address space (hex 100 to hex 0FFFF)
- 24-bit memory addresses (16 MB)
- Selection of data accesses (either 8-bit or 16-bit)
- 11 Interrupt levels
- Seven DMA channels
- I/O wait-state generation
- Arbitration for bus masters
- Refresh of system memory

2.2 Reference Documents

Consult the following documents for further information related to the AT-compatible bus:

- Technical Reference, Personal Computer AT, IBM #1502494 (©1984, IBM Corp.)
- APX 286 Hardware Reference Manual, Intel #210760-001 (©1983, Intel Corp.)
- Microsystem Components Handbook, Intel #230843-002 (©1985, Intel Corp.)

2.3 Bus Interface Lines and Signal Definitions

This section contains pin listings for the AT-compatible bus connectors. The signals carried on these connectors are also defined.

2.3.1 Connector Pin Listing

The AT-compatible bus connectors consist of eight 62-pin (top row) and six 36-pin (bottom row) edge connector sockets. The left-most connector position (P4/14) is the IBM PC/XT-compatible connector. This connector uses an 8-bit data bus. The remaining seven board positions are IBM PC/AT-compatible. These connectors use a 16-bit data bus.

NOTICE: Older DS3000 systems have six AT-compatible slots and two XT-compatible slots. Slots P4/14 and P5/15 are used as the XT-compatible slots.

Figure 2-1 shows the location of the AT-compatible bus connectors when there are two XT-compatible slots.

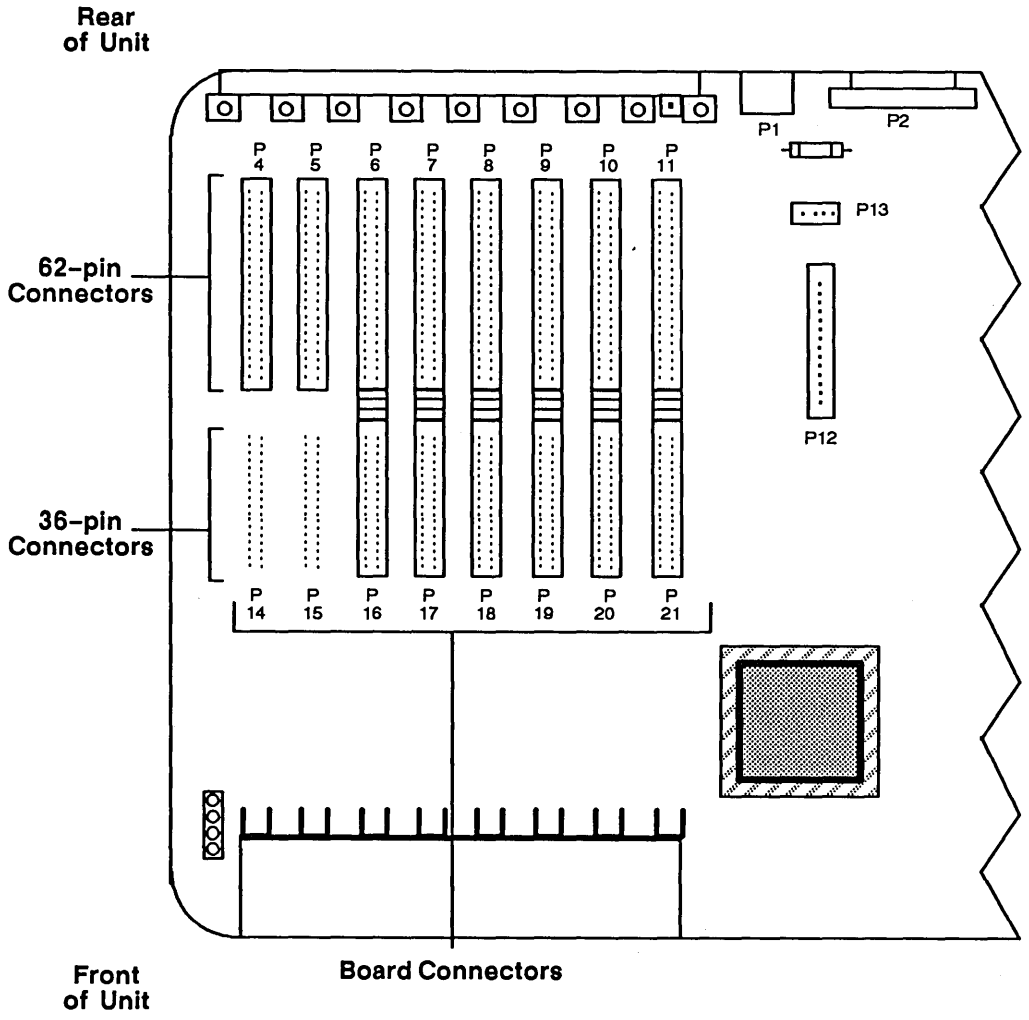


Figure 2-1. DS3000 Bus Connectors (Older Version)

NOTICE: In two positions on the AT-compatible bus, the 36-pin connector is not present (connectors P14 and P15). These positions can support only 62-pin IBM PC/XT-compatible bus adapters, servicing 8-bit data transfers. Newer DS3000 systems use P15 with P5 as a seventh AT-compatible slot. In these systems, P4 is the only XT-compatible slot (see Figure 2-2).

Figure 2–2 shows the location of the AT–compatible bus connectors on newer versions of the *Domain System*, when there is one XT–compatible slot.

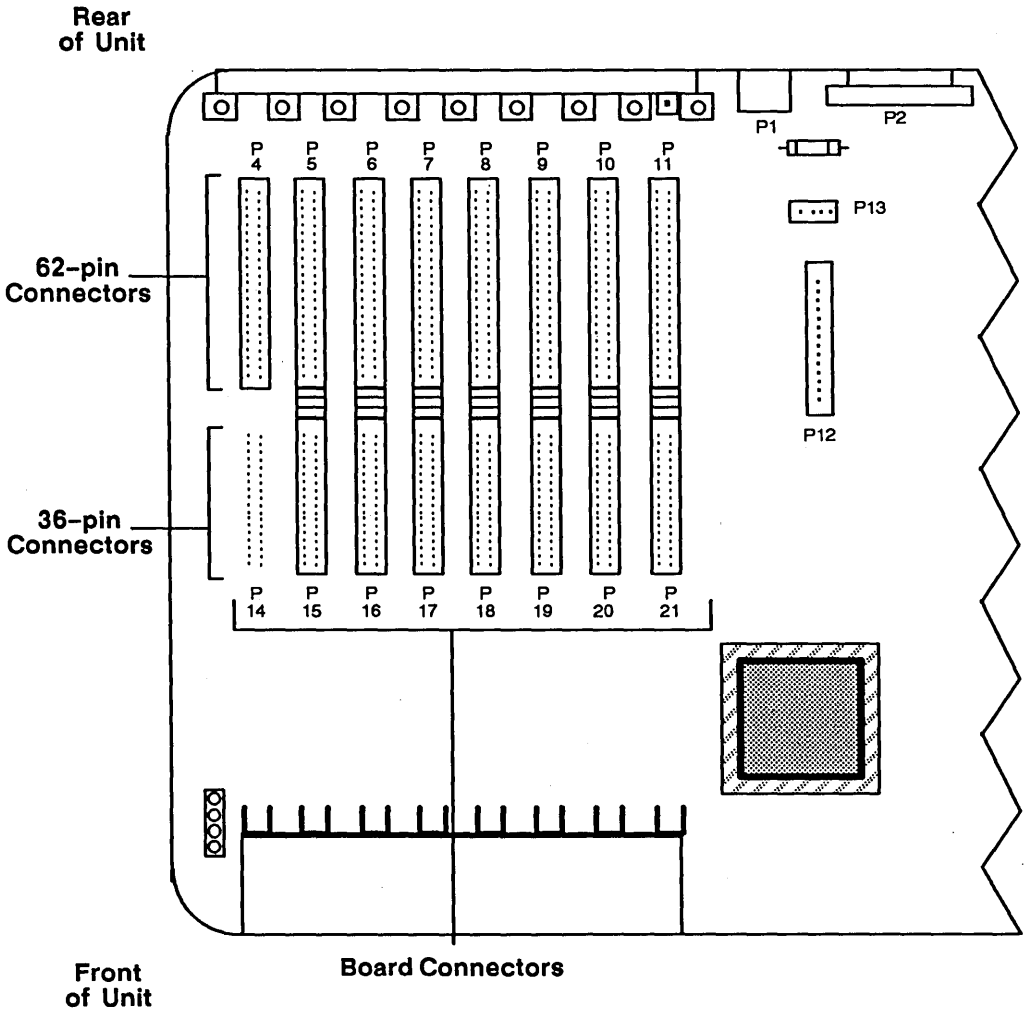


Figure 2–2. DS3000 and DS4000 Bus Connectors (Newer Version)

Table 2–1 lists the signals carried on the 62–pin P4 through P11 bus connectors.

Table 2–1. AT–Compatible Bus Signal List (Connectors P4 – P11)

Domain System Pin No.	IBM PC/AT Pin No.	I/O	Signal Name	Domain System Pin No.	IBM PC/AT Pin No.	I/O	Signal Name
1	A1	I	IO_CH_CK.L	2	B1	Ground	GND
3	A2	I/O	SD7	4	B2	O	RESET_DRV
5	A3	I/O	SD6	6	B3	Power	+5 V dc
7	A4	I/O	SD5	8	B4	I	IRQ9
9	A5	I/O	SD4	10	B5	Power	–5 V dc
11	A6	I/O	SD3	12	B6	I	DRQ2
13	A7	I/O	SD2	14	B7	Power	–12 V dc
15	A8	I/O	SD1	16	B8	I	OWS.L
17	A9	I/O	SD0	18	B9	Power	+12 V dc
19	A10	I	IO_CH_RDY	20	B10	Ground	GND
21	A11	O	AEN	22	B11	O	SMEMW.L
23	A12	I/O	SA19	24	B12	O	SMEMR.L
25	A13	I/O	SA18	26	B13	I/O	IOW.L
27	A14	I/O	SA17	28	B14	I/O	IOR.L
29	A15	I/O	SA16	30	B15	O	DACK3.L
31	A16	I/O	SA15	32	B16	I	DRQ3
33	A17	I/O	SA14	34	B17	O	DACK1.L
35	A18	I/O	SA13	36	B18	I	DRQ1
37	A19	I/O	SA12	38	B19	I/O	REFRESH.L
39	A20	I/O	SA11	40	B20	O	CLK
41	A21	I/O	SA10	42	B21	I	IRQ7
43	A22	I/O	SA9	44	B22	I	IRQ6
45	A23	I/O	SA8	46	B23	I	IRQ5
47	A24	I/O	SA7	48	B24	I	IRQ4
49	A25	I/O	SA6	50	B25	I	IRQ3
51	A26	I/O	SA5	52	B26	O	DACK2.L
53	A27	I/O	SA4	54	B27	O	TC
55	A28	I/O	SA3	56	B28	O	BALE
57	A29	I/O	SA2	58	B29	Power	+5 V dc
59	A30	I/O	SA1	60	B30	O	OSC
61	A31	I/O	SA0	62	B31	Ground	GND

Table 2-2 lists the signals carried on the 36-pin connectors (P15 through P21) bus connectors.

Table 2-2. AT-Compatible Bus Signal List (Connectors P15 - P21)

Domain System Pin No.	IBM PC/AT Pin No.	I/O	Signal Name	Domain System Pin No.	IBM PC/AT Pin No.	I/O	Signal Name
1	C1	I/O	SBHE.L	2	D1	I	MEM_CS16.L
3	C2	I/O	LA23	4	D2	I	IO_CS16.L
5	C3	I/O	LA22	6	D3	I	IRQ10
7	C4	I/O	LA21	8	D4	I	IRQ11
9	C5	I/O	LA20	10	D5	I	IRQ12
11	C6	I/O	LA19	12	D6	I	IRQ15
13	C7	I/O	LA18	14	D7	I	IRQ14
15	C8	I/O	LA17	16	D8	O	DACK0.L
17	C9	I/O	MEMR.L	18	D9	I	DRQ0
19	C10	I/O	MEMW.L	20	D10	O	DACK5.L
21	C11	I/O	SD8	22	D11	I	DRQ5
23	C12	I/O	SD9	24	D12	O	DACK6.L
25	C13	I/O	SD10	26	D13	I	DRQ6
27	C14	I/O	SD11	28	D14	O	DACK7.L
29	C15	I/O	SD12	30	D15	I	DRQ7
31	C16	I/O	SD13	32	D16	Power	+5 V dc
33	C17	I/O	SD14	34	D17	I	MASTER.L
35	C18	I/O	SD15	36	D18	Ground	GND

2.3.2 AT-Compatible Bus Signal Descriptions

This subsection contains descriptions of the CPU's AT-compatible bus signals. All signal lines are TTL-compatible. I/O adapters used with this bus should be designed with a maximum of two Low-power Schottky (LS) loads per line. Unless otherwise specified, the active (One) state of all signals is a voltage high (>2.4 volts) and the inactive (Zero) state of all signals is a voltage low (<0.5 volt). Signal names ending with an ".L" are the logical negation of this state structure (One = low and Zero = high).

After each signal name, the direction of the signal source is specified. An "I" (Input) after the signal name is an input to the system board or other bus Master, and therefore an output of the I/O adapter module or bus Slave. An "O" (Output) after the signal name is an output of the system board or other bus Master, and an input to the I/O adapter or bus Slave. Signals marked as (I/O) have bidirectional capability; either the bus Master or the bus Slave may be the source of the signal.

SA0 through SA19 (I/O)

Address bits 0 through 19 are used to address memory and I/O devices within the system. These 20 address lines, in addition to LA17 through LA23, are used to access up to 16 MB of memory. SA0 through SA19 gate on the system bus when BALE is high, and latch on the falling edge of BALE. These signals are generated by the system microprocessor or DMA controller. They also may be driven by other bus Masters or DMA controllers that reside on the I/O channel. Address bits SA0 through SA15 are used, in conjunction with the IOR.L and IOW.L control signals, to define transfers to the I/O address space.

LA17 through LA23 (I/O)

These signals (unlatched) are used to address memory and I/O devices within the system. When used with SA0 through SA19, they allow up to 16 MB of memory to be addressed. These signals are valid when BALE is high. LA17 through LA23 are not latched during microprocessor cycles, and therefore do not stay valid for the whole cycle. Their purpose is to generate memory decodes for memory cycles. These decodes are latched by I/O adapters on the falling edge of BALE. These signals may also be driven by other bus Masters or DMA controllers that reside on the AT-compatible bus. Note that these signals are decoded by the I/O adapter to generate MEM_CS16.L for 16-bit memory cycles.

CLK (O)

This is the 6-MHz (Series 3000) or 8-MHz (Series 4000) system clock. It is a synchronous microprocessor cycle clock with a cycle time of 167 nanoseconds at 6 MHz or 125 nanoseconds at 8 MHz. The clock has a 50% duty cycle. This signal should only be used for synchronization. It is not intended for applications that require a fixed frequency.

RESET_DRV (O)

Reset Drive is used to reset or initialize the system logic at power-up or during a low line-voltage outage. This signal is active high.

SD0 through SD15 (I/O)

These signals provide bus bits 0 through 15 for the microprocessor, memory, and I/O devices. SD0 is the least-significant bit and SD15 is the most-significant bit. All 8-bit devices on the AT-compatible bus use SD0 through SD7 to communicate with the microprocessor. All 16-bit devices use SD0 through SD15 to communicate with the microprocessor. To support 8-bit devices, the data on SD8 through SD15 is gated to SD0 through SD7 during 8-bit transfers to these devices. The 16-bit microprocessor transfers to 8-bit devices are converted to two 8-bit transfers. (For more information, see Subsection 2.4.1.)

BALE (O)

This signal is used on the system board to latch valid addresses and memory decodes from the microprocessor. It is available to the AT-compatible bus as an indicator of a valid microprocessor or DMA address (when used with AEN). CPU address bits SA0 through SA19 latch on the bus Master with the falling edge of BALE. BALE is forced high during DMA cycles. Note that BALE is used only by the I/O adapter to latch the LA17 through LA23 address lines (or to decode LA17 through LA23, indicating an address match for the I/O adapter). BALE may not occur on all 8-bit I/O cycles (which use only address lines SA0 through SA9 for device decoding) or on some 8-bit memory transfers. (For more information, see Subsection 2.4.1.)

IO_CH_CK.L (I)

I/O Channel Check provides the system board with parity (error) information about memory or devices on the AT-compatible bus. When this signal is active, it indicates an uncorrectable system error. In the DS3000, this signal asynchronously sets a flip-flop that causes a Non-Maskable-Interrupt (NMI) to occur. This provides an on-board register bit, which can be read and reset by the system software responsible for handling the device error.

IO_CH_RDY (I)

I/O Channel Ready is pulled low (not ready) by a memory or I/O device to lengthen bus cycles. Any slow device using this line should drive it low immediately upon detecting its valid address and a Read (or Write) command. Machine cycles are extended by an integral number of clock cycles (167 nanoseconds). This signal should be held low for no more than 2.5 microseconds. IO_CH_RDY should be driven by an open-collector or tri-state driver capable of sinking 20 mA.

IRQ0 through IRQ15 (I)
Interrupt Requests 3 through 7, 9 through 12, 14, and 15 are used to signal the microprocessor that an I/O device needs attention. Interrupt Requests 8 through 15 are slaved through IRQ2. An interrupt request is generated when an IRQ line is raised from low to high. The line must be held high until the microprocessor acknowledges the interrupt request to the device during the Interrupt Service routine.

The priority of IRQ8 through IRQ15 is actually higher than IRQ4 through IRQ7 because IRQ8 through IRQ15 are in the second PIC, which is slaved to the Master at IRQ2. Note that IRQ13 is not available on the bus. In the DS3000, it is connected to Output Port Bit 7 of the 2681 SIO chip and is used by diagnostics to verify the integrity of the interrupt controllers. Table 2–3 lists the interrupt request priorities.

Table 2–3. Interrupt Request Priorities

IRQ No.	Interrupt Priority	Interrupt Controller	8– or 16–Bit Bus	Domain System Function
IRQ0 *	1	1	CPU	MC6840 Timer
IRQ1 *	2	1	CPU	2681 SIO Port 1
IRQ3	3	1	CPU	Network Board or User Device
IRQ2 *	–	1	8	Cascaded Slave PIC to Master (IRQ8 – IRQ15)
IRQ8 *	4+1	2	CPU	MC146818 Calendar
IRQ9	4+2	2	8	802.3 Network Controller–AT #2, SPE Serial Line 2, or User Device
IRQ10	4+3	2	16	802.3 Network Controller–AT #1 or User Device
IRQ11	4+4	2	16	PC Coprocessor or User Device
IRQ12	4+5	2	16	User Device
IRQ13 *	4+6	2	CPU	Used During Diagnostic Tests
IRQ14	4+7	2	16	Winchester Drive or User Device
IRQ15	4+8	2	16	PC Coprocessor Alternate or User Device
IRQ4	5	1	8	SPE Board Serial Line 1 or User Device
IRQ5	6	1	8	Tape Drive or User Device
IRQ6	7	1	8	Floppy Drive or User Device
IRQ7	8	1	8	SPE Board Parallel Port or User Device

* Used on-board CPU. Not available on the Bus.

If an optional device is not present in the *Domain System* , the Interrupt Request line reserved for that device may be assigned to another device.

IOR.L (I/O)
I/O Read instructs an I/O device to drive its data onto the data bus. It may be driven by the system microprocessor (or DMA controller), or by a bus Master (or DMA controller) that is resident on the AT–compatible bus. This signal is active low.

IOW.L (I/O)
I/O Write instructs an I/O device to read the data on the data bus. It may be driven by any bus Master or DMA controller in the system. This signal is active low.

SMEMR.L (O) MEMR.L (I/O)
These signals instruct the memory devices to drive data onto the data bus. SMEMR.L is active only when the memory decode is within the lower 1 MB of memory space. MEMR.L is active on all memory read cycles. MEMR.L may be driven by any bus Master or DMA controller in the system. SMEMR.L is derived from MEMR.L and the decode of the lower 1 MB of memory. When a bus Master on the AT–compatible bus wishes to drive MEMR.L, it must have the address lines valid on the bus for one system clock period before driving MEMR.L active. Both signals are active low.

SMEMW.L (O) MEMW.L (I/O)

These signals instruct the memory devices to store the data present on the data bus. SMEMW.L is active only when the memory decode is within the lower 1 MB of the memory space. MEMW.L is active on all memory write cycles. MEMW.L may be driven by any bus Master or DMA controller in the system. SMEMW.L is derived from MEMW.L and the decode of the lower 1 MB of memory. When a bus Master on the AT-compatible bus wishes to drive MEMW.L, it must have the address lines valid on the bus for one system clock period before driving MEMW.L active. Both signals are active low.

DRQ0 through DRQ7 (I)

DMA Requests 0 through 3 and 5 through 7 are asynchronous channel requests used by peripheral device controllers or bus Masters to gain DMA service or bus mastership. They are prioritized, with DRQ0 having the highest priority and DRQ7 having the lowest priority. A request is generated by bringing a DRQ line to an active level. A DRQ line must be held high until the corresponding DMA Request Acknowledge (DACK) line goes active. DRQ0 through DRQ3 perform 8-bit DMA transfers; DRQ5 through DRQ7 perform 16-bit transfers. DRQ4 is used on the system board to cascade Channels 0 through 3 (see Table 2-4) for the DMA Request priorities. It is not available on the AT-compatible bus. Table 2-4 lists the DMA Request priorities for the bus.

Table 2-4. DMA Request Priorities

DRQ No.	DMA Priority	8- or 16-Bit Transfer	DMA Controller	Domain System Function
DRQ0	1	8	1	User Device
DRQ1	2	8	1	Tape Drive or User Device
DRQ2	3	8	1	Floppy Drive or User Device
DRQ3	4	8	1	802.3 Network Controller-AT #2 or User Device
DRQ4 *	–	–	2	Cascade for Channels 0 - 3
DRQ5	5	16	2	PC Coprocessor or User Device
DRQ6	6	16	2	802.3 Network Controller-AT #2 or User Device
DRQ7	7	16	2	Reserved for Winchester

* DMA Channel 4 is used to cascade Channels 0 through 3 and is not available on the bus.

If an optional device is not present, the DMA channel reserved for that device may be asssigned to another device.

DACK0.L through DACK3.L and DACK5.L through DACK7.L (O)

DMA Acknowledge 0 through 3 and 5 through 7 are used to acknowledge DMA requests (DRQ0 through DRQ7). They are active low.

AEN (O)

Address Enable unlatches the microprocessor and other devices from the AT-compatible bus and allows DMA transfers to take place. When this line is active, the DMA controller has control of the address bus and the data bus READ and WRITE command lines (memory and I/O). This line is forced low when a bus Master assumes control of the bus.

REFRESH.L (I/O)

This signal indicates a refresh cycle and is driven by a bus Master on the I/O channel.

TC (O)
Terminal Count provides a pulse when the terminal count for any DMA channel is reached.

SBHE.L (I/O)
Bus High Enable indicates a transfer of data on the upper byte of the data bus, SD8 through SD15. The Sixteen-bit devices use SBHE.L to condition data bus buffers tied to SD8 through SD15.

SBHE.L and SA0 Encodings (for 16-Bit Devices)

SBHE.L	SAO	Function
0	0	Word Transfer
0	1	Byte Transfer on SD8 through SD15
1	0	Byte Transfer on SD0 through SD07
1	1	Reserved

Note that for 8-bit transfers, SA0 is the least-significant address bit that defines whether an odd or even byte is being transferred on data bits SD0 through SD7. SBHE.L has no meaning for 8-bit devices and may be either high or low.

MASTER.L (I)
This signal is used with a DRQ line to gain control of the system. A bus Master on the AT-compatible bus issues a DRQ to a DMA channel, which has been programmed into cascade mode, and receives a DACK. Upon receiving the DACK, an I/O bus Master may pull MASTER.L low, which allows it to control the system address, data, and control lines (a condition known as tri-state). After MASTER.L is low, the I/O bus Master must wait one system clock period before driving the address and data lines, and two clock periods before issuing a Read or Write command. If this signal is held low for more than 15 microseconds, the system memory may be lost because no refresh is performed during that time.

MEM_CS16.L (I)
MEM16 Chip Select signals the system board if the present data transfer is a 16-bit memory cycle. It is derived from the decode of LA17 through LA23. This requires all 16-bit memory devices to occupy at least 128 KB of address space on the AT-compatible bus. It also requires that the device does not decode the SA address lines as a condition to driving MEM_CS16.L because the SA lines are not valid in time to meet the MEM_CS16.L timing requirements. MEM_CS16.L should be driven with an open-collector or tri-state driver capable of sinking 20 mA.

IO_CS16.L (I)
I/O 16-Bit Chip Select signals the system board that the present data transfer is a 16-bit I/O cycle. It is derived from an address decode of SA0 through SA15. IO_CS16.L is active low and should be driven with an open-collector or tri-state driver capable of sinking 20 mA.

OSC (O)
Oscillator (OSC) is a high-speed clock with a 70-nanosecond period (14.31818 MHz). This signal is not synchronous with the system clock. It has a 50% duty cycle.

OWS.L (I)
The Zero Wait State (OWS.L) signal tells the microprocessor that it can complete the present bus cycle without inserting any additional wait cycles. To run a memory cycle to a 16-bit device without wait cycles, OWS.L is derived from an address decode gated with a Read or Write command. To run a memory cycle to an 8-bit device with a minimum of two wait states, OWS.L should be driven active one system clock

after the Read or Write command is active-gated with the address decode for the device. Memory Read and Write commands to an 8-bit device are active on the falling edge of the system clock. OWS.L must be synchronous to the system clock (CLK) and meet specific setup and hold timing requirements to prevent system malfunction (see Subsection 2.4.2). OWS.L is active low and should be driven with an open-collector or tri-state driver capable of sinking 20 mA.

2.4 Protocol

Subsections 2.4.1 through 2.4.9 describe the various types of data transfers and related processes that take place on the bus.

2.4.1 16-Bit vs. 8-Bit Data Transfers

The bus activity that occurs for 16-bit devices is different than for 8-bit devices. To determine the kind of cycle that occurs, two signal lines (MEM_CS16.L and IO_CS16.L) are available to 16-bit devices that enable the bus Master to perform appropriately. These two signals affect the timing of the bus cycle and generate a 1 wait-state cycle for 16-bit devices and a 4 wait-state cycle for 8-bit devices if no IO_CH_RDY response is given by the device. This is typically the fastest cycle time available to the device (except for those devices that can assert the OWS signal). Devices can slow down cycles (insert wait states) by deasserting the IO_CH_RDY signal (make it not-ready or low) for the appropriate period.

Transfers to 16-bit devices can occur over either the low-order byte (SD0 through SD7) or the high-order byte (SD8 through SD15) or both as indicated by signals SA0 and SBHE.L (see the signal definitions in Subsection 2.3.2). Word or longword transfers must be word-aligned (started on an even byte address).

Transfers to 8-bit devices occur over the low-order byte only (SD0 through SD7). The MC68020 processor in the DS3000 can execute instructions that cause a 16-bit data transfer to 8-bit devices. When this occurs, the MC68020 sends two 8-bit transfers over the low-order byte (SD0 through SD7). The MC68020 can send long, short, or byte transfers to 8-bit or 16-bit devices.

2.4.2 Wait States

Two signals (IO_CH_RDY and OWS.L) are available to generate faster or slower bus cycles as needed by particular I/O adapters. The IO_CH_RDY signal is used by devices that need to produce more wait states than the nominal 1 for 16-bit designs or 4 for 8-bit designs.

The OWS.L signal can be used to speed up memory cycles by reducing the number of wait states taken during the bus cycle. For 16-bit devices, the number of wait states can be reduced from 1 to 0. For 8-bit devices, the number can be reduced from 4 to a lower number, depending on the time that OWS.L is driven low.

The timing requirements on OWS.L are much more restrictive than for IO_CH_RDY because the setup and hold times must be met or the processor will malfunction. The IO_CH_RDY signal does not have these restrictions since the signal is passed through a synchronizer. It must meet timing requirements to generate the proper number of wait states, but the timing is easier to meet. The system will not malfunction through metastability faults if the timing is not met.

Most devices use the nominal number of wait states and do not need to drive either signal. Devices that cannot guarantee a response generate wait states by using IO_CH_RDY. Those devices that affect system throughput through high utilization, or that have other timing restrictions can generate fewer wait states by using the OWS.L signal.

2.4.3 Read Cycles

A read cycle consists of the following steps:

1. The Master transmits address lines SA0 through SA19 via a latch controlled by BALE and latches them on the trailing edge of BALE. Address lines LA17 through LA23 are sent before BALE is high, but are not latched on the Master's board. All address lines become valid when BALE is high, but SA0 through SA19 continue valid (until a new BALE cycle begins) while LA17 through LA23 become invalid after BALE returns low. If necessary, the I/O adapter latches the LA address lines on the falling edge of BALE (for memory cycles only, LA address lines are not used during I/O cycles). SBHE.L is activated by the Master if a data transfer takes place on the upper byte (SD8 through SD15) of the data bus.
2. The Master activates one of three control signals (MEMR.L, SMEMR.L, or IOR.L) to make the Slave device place the data on the data bus. MEMR.L is asserted on all memory read cycles, SMEMR.L is asserted on all memory read cycles in the lower 1 MB of memory space, and IOR.L is asserted on all read cycles in the I/O address space.
3. The addressed Slave responds by asserting either OWS.L or IO_CH_RDY (see Subsection 2.4.2 for a detailed discussion). The length of time that these signals are asserted will determine the number of wait states for the bus cycle. If no response is given (neither OWS.L nor IO_CH_RDY are driven low), a 1 wait-state cycle will automatically occur on 16-bit transfers and a 4 wait-state cycle will automatically occur on 8-bit transfers.
4. The Master deactivates the LA address lines (after the falling edge of BALE), independent of the Slave's response time.
5. The addressed Slave responds to the control signal issued in Step 2 by placing the data on the data bus.
6. The addressed Slave removes its response signal (OWS.L or IO_CH_RDY) in time to terminate with the correct number of wait states.
7. The Master captures the data on the data bus and deactivates its control signal.
8. The Slave removes the data from the data bus.

2.4.4 Write Cycles

A write cycle consists of the following steps:

1. The Master transmits the address lines SA0 through SA19 through a latch controlled by BALE and latches them on the trailing edge of BALE. Address lines LA17 through LA23 are sent before BALE is high, but are not latched on the Master's board. All address lines become valid when BALE is high, but SA0 through SA19 continue valid (until a new BALE cycle begins) while LA17 through LA23 become invalid after BALE returns low. If necessary, the I/O Adapter latches the LA address lines on the falling edge of BALE (for memory cycles only, LA address lines are not used during I/O cycles). SBHE.L is activated by the Master if a data transfer takes place on the upper byte (SD8 through SD15) of the data bus.
2. The Master places the data on the data bus.
3. The Master activates one of three control signals (MEMW.L, SMEMW.L or IOW.L) to tell the Slave device that the Master has placed its data on the data bus:

   MEMW.L is asserted on all memory write cycles, SMEMW.L is asserted on all memory Write cycles in the lower 1 MB of memory space, and IOW.L is asserted on all write cycles in the 64 KB I/O address space.
4. The Master deactivates the LA address lines (after the falling edge of BALE), independent of the Slave's response time.

5. The addressed Slave asserts either OWS.L or IO_CH_RDY (see Subsection 2.3.2 for a detailed discussion). The length of time that these signals are asserted will determine the number of wait states for this bus cycle. If no response is given (neither OWS.L nor IO_CH_RDY are driven low), a 1 wait-state cycle will automatically occur on 16-bit transfers and a 4 wait-state cycle will automatically occur on 8-bit transfers.

6. The addressed Slave removes its response signal (OWS.L or IO_CH_RDY) in time to terminate with the correct number of wait states.

7. The Master deactivates its control signal and the Slave captures the data presented on the data bus (on or before the Master deactivates its control signal).

8. The Master removes the data from the data bus.

2.4.5 Direct Memory Access Cycles

Direct Memory Access (DMA) cycles are implemented by using two cascaded Intel 8237A-5 DMA controller chips, which provide four channels of DMA for each chip. Of the eight possible channels, one is used in cascading and seven are available to the AT-compatible bus.

One of the DMA Controllers contains Channels 0 through 3, which support 8-bit data transfers between 8-bit I/O adapters and 8- or 16-bit memory on the AT-compatible bus. Each channel transfers data throughout the 16-MB system address space in 64-KB blocks (maximum).

The second DMA Controller contains Channels 4 through 7. Channel 4 is used to cascade Channels 0 through 3 to the system processor. Channels 5 through 7 support 16-bit data transfers between 16-bit I/O adapters and 16-bit system memory. These DMA channels transfer data throughout the 16-MB system address space in 128-KB blocks (maximum). Channels 5 through 7 cannot transfer data on odd byte boundaries.

The following protocol is used to implement a DMA cycle (assume that the DMA controller chips were previously programmed with the appropriate data for each channel):

1. A DMA cycle is generated by asserting a DMA Request line (DRQx raised high) until the corresponding DMA Request Acknowledge is received (DACKx.L is asserted low). If only one data transfer is desired, DRQx is then deasserted. The DRQx, internally on the system board, sends a hold request to the system processor. When the processor that issues a Hold Acknowledge grants the Hold Request, AEN is asserted, the DACKx.L is given, and the cycle proceeds.

2. AEN is asserted to degate other I/O devices from the bus. This makes the bus address, data, and control signals available to the DMA controller and the requesting device. AEN remains asserted throughout the DMA cycle.

3. The memory address (SA0 through SA19 and LA17 through LA23) is available to the bus throughout the remainder of the cycle. BALE is also asserted throughout the entire cycle, unlike during other (normal) memory cycles.

4a. For a DMA memory read cycle, MEMR.L and SMEMR.L are asserted (if the address is within the first MB). The memory accesses the data and places it on the data bus. IOW.L is then asserted to write the data to the device receiving the DACKx.L.

4b. For a DMA memory write cycle, IOR.L is asserted. The device receiving the DACKx.L accesses the data and places it on the data bus. MEMW.L and SMEMW.L are then asserted to write the data to the addressed memory location (if the address is within the first MB).

5. If the request (DRQx) is still asserted, another cycle will occur, as in Steps 3 and either 4a or 4b, with the memory address incrementing or decrementing as programmed in the controller. Otherwise, the cycle ends with all bus signals being released in the proper order.

2.4.6 Refresh Cycles

The system board provides refresh cycles to the bus at regular intervals (approximately 15 microseconds) to refresh all of the system's dynamic memory on the system board and for any memory included in I/O adapters. A state machine, driven by a timebase, provides this capability, inserting refresh cycles on the AT-compatible bus. The refresh cycle protocol is as follows:

1. When the timer interval expires, the BALE, AEN, and REFRESH.L signals are all asserted as the refresh cycle begins. At the completion of the refresh cycle, the REFRESH.L signal increments the refresh address.
2. The state machine sequentially places the address on the bus (SA0 through SA7), and issues the MEMR.L and SMEMR.L signals at each CLK signal.
3. All bus devices with the appropriate logic allow a refresh cycle to occur. If any I/O adapter in the system lowers IO_CH_RDY, the cycle will continue in this state until IO_CH_RDY is raised.
4. Two CLK cycles after IO_CH_RDY comes high, MEMR.L and SMEMR.L are deasserted. After this, REFRESH.L, the address lines, BALE, and AEN are deasserted and the refresh cycle ends.

2.4.7 Bus Mastership Arbitration

An I/O adapter obtains mastership of the bus by asserting its DMA Request signal (DRQx) to a DMA channel that has been programmed in cascade mode, and then asserting the MASTER.L signal after its DMA Acknowledge is received (the system board asserts DACKx.L). At this point, the system processor relinquishes ownership of the bus. The MASTER.L signal prevents assertion of the AEN signal, allowing the bus Master to comunicate with the I/O devices. Programming a DMA channel into cascade mode prevents the DMA controllers from driving the address and control bus, making the bus available to the bus Master. The I/O adapter now has full ownership of the bus until it releases the DRQx and MASTER.L signals. Note that ownership implies responsibility for bus timing, concern for refresh of system memory, the disabling of all other DMA activity, and other system issues.

In the Series 4000, an alternate method of bus arbitation exists that implements a Master Request Register. By setting a particular bit in this register, an external processor asserts its DMA Request signal to the system processor. The address translation map in the Series 4000 restricts external Masters to transfers of 512 KB to or from main memory. This map also allows the DMA controllers to view memory as a contiguous address space.

2.4.8 Interrupts

Interrupts are implemented using two cascaded Intel 8259A Programmable Interrupt Controller (PIC) chips. Of the 16 possible interrupts, one is used for cascading, four are used internally by the system processor, and 11 are available on the AT-compatible bus (see Table 2-3).

Interrupt vectors are preprogrammed by system software for each of the interrupt channels into registers in the PICs. A device requests an interrupt by raising its Interrupt Request line (IRQx) from low to high and keeping it held high until acknowledged by software in the interrupt service routine.

Interrupts are typically implemented in an I/O adapter with registers that are read and/or written by I/O accesses over the AT-compatible bus. The interrupt line is typically one of the bits in a register that is set asynchronously by the device (event) needing the interrupt. During the execution of the interrupt service routine for that level, the register would be accessed to discover the reason for the interrupt, and the interrupt bit itself would be turned off, thus completing the interrupt cycle in a hardware sense. The software takes further action as appropriate.

2.4.9 Initialization

The RESET_DRV signal is derived from the POWER GOOD signal provided by the *Domain System* power supply in the system unit. It is used to initialize system devices at power-up and to reset those devices if either ac and/or dc voltages become too low for proper system operation.

When the supply is turned off for a minimum of 1 second and then switched back on, the POWER GOOD signal is given. This signal is a logical AND of the ac sense signal and the dc output sense signals within the power supply.

The ac sense signal forces POWER GOOD low (off) at least 500 microseconds in the Series 3000 and 2 milliseconds in the Series 4000 before any output voltage falls below specified limits. The reference for measuring these time periods is minimum line voltage and maximum load.

The dc output sense signals hold POWER GOOD low (off) when power is applied until all outputs are at the minimum sense levels. This POWER GOOD turn-on delay is 100 milliseconds minimum and 500 milliseconds maximum.

The RESET_DRV signal is the opposite polarity of the POWER GOOD signal from the supply. That is, if the power is indicated not good, the POWER GOOD signal is low and the RESET_DRV signal is high.

2.5 Bus Signal Timing

Appendix A of this manual contains timing diagrams and a list of cycle times that illustrate the AT-compatible bus signal timing waveforms and the related timing parametric information.

2.6 Bus Voltage Level Requirements

Standard Low-power Schottky (LS) and ALS voltage levels are used for all signals. These are defined as:

Output Voltages	Input Voltages
VOH = 2.4 volts minimum	VIH = 2.0 volts minimum
VOL = 0.5 volt maximum	VIL = 0.8 volt maximum

These levels are considered to be worst-case levels under all loading and environmental conditions. Signal polarity (active/inactive, One/Zero, high/low, etc.) is defined for each signal in Subsection 2.3.2.

2.7 Bus Electrical Interface Circuitry

Any circuitry that meets the voltage level, loading, timing, and other conditions described in this chapter can be used to interface to the AT-compatible bus. The following circuits have been used successfully and are recommended:

Drivers: 74ALS244A

Receivers: Any LS or ALS circuits otherwise meeting this specification

Transceivers: 74ALS245A

Octal Register and Bus Driver: 74ALS573

2.8 Bus Electrical Loading

Since there are nine total bus locations (eight I/O adapters plus the system board), we can define two LS TTL loads per location (for a total of 18) and still use 74LS245 compatible circuitry.

2.9 Bus Electrical Termination

The bus is entirely contained within the *Domain System* unit, is not intended to be extended, and is driven by tri-state LS TTL circuits. Therefore, for most signals, the bus is not terminated with any line matching impedance. All I/O adapter circuit boards should be designed to minimize bus signal lengths and reduce signal reflections and cross talk. Bus loading should generally be limited to one or two LS TTL loads.

Some signals are terminated with a resistor on the system board to define the undriven default state for I/O adapters that are capable of assuming bus mastership (e.g., switch-over time for DMA). Do not activate the signal or use open collector drivers. It is never necessary for an I/O adapter to provide a terminating impedance for the AT-compatible bus.

Table 2-5 lists terminated signals. Except for those listed here, all signals are unterminated.

Table 2-5. Terminated Signals

Signal Name	Terminating Resistor	Terminating Voltage (V dc)
MEMR.L	10K ohm	+5
MEMW.L	10K ohm	+5
SMEMR.L	10K ohm	+5
SMEMW.L	10K ohm	+5
IOR.L	10K ohm	+5
IOW.L	10K ohm	+5
IO_CH_CK.L	4.7K ohm	+5
IO_CH_RDY	1K ohm	+5
MASTER.L	300 ohm	+5
MEM_CS16.L	300 ohm	+5
OWS.L	300 ohm	+5
IO_CS16.L	300 ohm	+5
REFRESH.L	5K ohm	+5
AEN	1K ohm	+5
BALE	1K ohm	+5
SBHE.L	1K ohm	+5

2.10 Physical Address Space

Table 2–6 lists the physical address space allocation for the DS3000 system.

Table 2–6. 16–MB Physical Address Space Allocation

Physical Address Range	DS3000 Device
000000 – 007FFF	BOOT PROM
008000 – 0080FF	CPU STATUS REGISTER
008100 – 0081FF	CPU CONTROL REGISTER
008200 – 0083FF	NOT USED
008400 – 0087FF	SIO
008800 – 0088FF	INTERVAL TIMER
008900 – 0089FF	CALENDAR
009000 – 0090FF	DMA CONTROLLER #1
009100 – 0091FF	DMA CONTROLLER #2
009200 – 0092FF	DMA PAGE REGISTER
009300 – 0093FF	LATCH–PAGE–ON–PARITY–ERROR REGISTER
009400 – 0094FF	INTERRUPT CONTROLLER #1
009500 – 0095FF	INTERRUPT CONTROLLER #2
009600 – 03FFFF	NETWORK ID PROM
040000 – 05FFFF	AT–COMPATIBLE BUS I/O SPACE (See Table 2–7)
060000 – 07FFFF	NOT USED
080000 – 09FFFF	AT–COMPATIBLE BUS MEMORY SPACE
0A0000 – 0BFFFF	COLOR OR ALTERNATE MONO GRAPHICS MEMORY SPACE
0C0000 – 0DFFFF	ALTERNATE MONO GRAPHICS MEMORY SPACE
0E0000 – 0FFFFF	ALTERNATE COLOR GRAPHICS MEMORY SPACE
100000 – 1FFFFF	MAIN MEMORY (FIRST MB)
200000 – 2FFFFF	MAIN MEMORY (SECOND MB)
300000 – 3FFFFF	MAIN MEMORY (THIRD MB)
400000 – 4FFFFF	MAIN MEMORY (FOURTH MB)
500000 – 5FFFFF	MAIN MEMORY (FIFTH MB)
600000 – 6FFFFF	MAIN MEMORY (SIXTH MB)
700000 – 7FFFFF	MAIN MEMORY (SEVENTH MB)
800000 – 8FFFFF	MAIN MEMORY (EIGHTH MB)
900000 – 91FFFF	AT–COMPATIBLE BUS MEMORY SPACE
920000 – BFFFFF	AT–COMPATIBLE BUS MEMORY SPACE
C00000 – CFFFFF	PC COPROCESSOR
D00000 – DFFFFF	PC COPROCESSOR ALTERNATE
FA0000 – FDFFFF	MONO GRAPHICS MEMORY SPACE
FE0000 – FFFFFF	AT–COMPATIBLE BUS MEMORY SPACE

Table 2–7 lists the physical address space allocation for the AT–compatible bus I/O devices used in the DS3000.

Table 2–7. Physical Address Allocation Within AT–Compatible Bus I/O Space

DS3000 Physical Address Range	AT–Compatible Bus Physical Address Range	DS3000 AT–Compatible Bus Devices
040000 – 047C07	000 – 0FF	Reserved
047C08 – 04CC07	100 – 19F	Unused
04D000 – 04D007	1A0 – 1A7	Winchester
04D400 – 04FFFF	1A8 – 210	Unused
050000 – 050F80	218 – 21F	Tape Drive
051000 – 051C07	220 – 23F	Network Interface
052000 – 057B80	240 – 2F7	Unused
057C00 – 057F80	2F8 – 2FF	SPE Board Serial Line 2 (SIO3)
058000 – 058800	300 – 310	802.3 Network Controller–AT
059000 – 059C07	320 – 33F	Network Interface
05BC00 – 05BF80	378 – 37F	SPE Board Parallel Line
05C000 – 05D407	380 – 3AF	Unused
05D800 – 05DC07	3B0 – 3BF	Alternate Color or Monochrome Graphics
05E000 – 05E407	3C0 –3CF	Unused
05E800 – 05EC07	3D0 –3DF	Alternate Monochrome or Color Graphics
05F000 – 05F780	3E0 – 3EF	Unused
05F800 – 05F807	3F0 – 3F7	Floppy Interface
05FC00 – 05FF80	3F8 – 3FF	SPE Board Serial Line 1 (SIO2)

Table 2–8 lists the physical address space allocation for the DS4000 system.

Table 2–8. 64–MB Physical Address Space Allocation

Physical Address Range	DS4000 Device
000000 – 00FFFF	BOOT PROM
010000 – 0100FF	CPU STATUS REGISTER
010100 – 0101FF	CPU CONTROL REGISTER
010200 – 0102FF	CACHE CONTROL REGISTER
010300 – 0103FF	TASK ALIAS REGISTER
010400 – 0104FF	SIO1
010500 – 0105FF	SIO2
010800 – 0108FF	INTERVAL TIMER
010900 – 0109FF	CALENDAR
010C00 – 010CFF	DMA CONTROLLER #1
010D00 – 010DFF	DMA CONTROLLER #2
011000 – 0110FF	INTERRUPT CONTROLLER #1
011100 – 0111FF	INTERRUPT CONTROLLER #2
011200 – 0112FF	NETWORK ID PROM
011300 – 0113FF	LATCH–PAGE–ON–PARITY–ERROR REGISTER
011600 – 0116FF	MASTER REQ REGISTER
012000 – 013FFF	CACHE RAM
014000 – 015FFF	CACHE CONDITION CODE RAM
016400 – 0164FF	SELECTIVE CLEAR LOCATIONS
017000 – 0177FF	ADDRESS TRANSLATION MAP
040000 – 05FFFF	AT–COMPATIBLE BUS I/O SPACE
060000 – 07FFFF	NOT USED
080000 – 09FFFF	AT–COMPATIBLE BUS MEMORY SPACE
0A0000 – 0BFFFF	COLOR OR ALTERNATE MONO GRAPHICS MEMORY SPACE
0C0000 – 0DFFFF	ALTERNATE MONO GRAPHICS MEMORY SPACE
0D0000 – 0DFFFF	NETWORK BOOT PROM (In place of alternate mono graphics memory space)
0E0000 – 0EFFFF	ALTERNATE NETWORK BOOT PROM (In place of alternate color graphics memory space)
0E0000 – 0FFFFF	ALTERNATE COLOR GRAPHICS MEMORY SPACE
120000 – FBFFFF	AT–COMPATIBLE BUS MEMORY SPACE
FA0000 – FDFFFF	MONO GRAPHICS MEMORY SPACE
FE0000 – FFFFFF	AT–COMPATIBLE BUS MEMORY SPACE
1000000 – 1FFFFFF	MAIN MEMORY (FIRST 16 MB)
2000000 – 2FFFFFF	MAIN MEMORY (SECOND 16 MB)
3000000 – 3FFFFFF	NOT USED

Table 2-9 lists the physical address space allocation for the AT-compatible bus I/O devices used in the DS4000.

Table 2-9. Physical Address Allocation Within AT-Compatible Bus I/O Space

Series 4000 Physical Address Range	AT-Compatible Bus Physical Address Range	DS4000 AT-Compatible Bus Devices
040000 - 047C07	000 - 0FF	Reserved
047C08 - 04CC07	100 - 19F	Unused
04D000 - 04D007	1A0 - 1A7	Winchester
04D400 - 04FFFF	1A8 - 210	Unused
050000 - 050F80	218 - 21F	Tape Drive
051000 - 051C07	220 - 23F	Network Interface
052000 - 057B80	240 - 2F7	Unused
057C00 - 057F80	2F8 - 2FF	SPE Board Serial Line 2 (SIO4)
058000 - 058800	300 - 310	802.3 Network Controller-AT
059000 - 059C07	320 - 33F	Network Interface
05BC00 - 05BF80	378 - 37F	SPE Board Parallel Line
05C000 - 05D407	380 - 3AF	Unused
05D800 - 05DC07	3B0 - 3BF	Alternate Color or Monochrome Graphics
05E000 - 05E407	3C0 - 3CF	Unused
05E800 - 05EC07	3D0 - 3DF	Alternate Monochrome or Color Graphics
05F000 - 05F780	3E0 - 3EF	Unused
05F800 - 05F807	3F0 - 3F7	Floppy Interface
05FC00 - 05FF80	3F8 - 3FF	SPE Board Serial Line 1 (SIO5)

2.11 DS3000 and DS4000 Power Allocation

Table 2–10 lists the power allocation for the DS3000 workstation.

Table 2–10. DS3000 Power Allocation

System Component	Power Consumption (Amps)			
	+5 V	–5 V	+12 V	–12 V
System Unit (CPU, DMMU, and 2–MB Memory)	8.0			
Apollo Token Ring (two–board set)	3.0	0.05	0.1	0.1
2–MB Expansion Memory (two–board set)	1.0			
2–MB Expansion Memory (single board)	0.3			
Winchester Disk Drive (72 MB)	1.5		2.5	
Winchester Disk Drive (155 MB)	1.5		2.5	
Winchester Disk Drive (348 MB)	1.5		2.5	
Floppy Disk Drive	0.8		0.5	
Color Display Controller	3.0			
Winchester/Floppy Disk Controller (72 MB)	1.3			
Winchester/Floppy Disk Controller (155 MB and 348 MB)	1.3			
Tape Cartridge Drive	0.6		2.4	
Tape Drive Controller	1.5		0.1	
Monochrome Display Controller	2.2	0.05		
802.3 Network Controller–AT	1.7		0.4	
Serial/Parallel Controller	0.7		0.05	0.05
PC Coprocessor Board	2.8			
Maximum Power Available	24.0 A	0.5 A	6.0 A	0.5 A

Table 2-11 lists the power allocation for the DS4000 workstation.

Table 2-11. DS4000 Power Allocation

System Component	Power Consumption (Amps)			
	+5 V	-5 V	+12 V	-12 V
System Unit (CPU, PMMU, and 8-MB Memory)	8.50			
Apollo Token Ring Network Controller-AT	1.85	0.012	0.08	0.06
4-MB Memory Board	0.25			
8-MB Memory Board	0.50			
Winchester Disk Drive (155 Mb)	1.50		2.50	
Winchester Disk Drive (348 Mb)	1.50		2.50	
Floppy Disk Drive	0.80		0.50	
8-Plane Color Display Controller	2.50			
Winchester/Floppy Disk Controller (OMTI 8621)	1.30			
Tape Cartridge Drive	0.60		2.40	
Tape Drive Controller	1.50		0.10	
8-MHz Monochrome Display Controller	2.20	0.05		
802.3 Network Controller-AT	1.70		0.40	
Serial/Parallel Controller	0.70		0.050	0.050
PC Coprocessor Board	2.80			
Maximum Power Available	40.0 A	0.75 A	6.0 A	0.75 A

2.12 Safety Requirements

This section contains a list of safety requirements that must be considered when adding printed circuit boards to the AT-compatible bus.

- The printed circuit board must be able to accept up to 42.4 volts at 8 amps.
- The printed circuit board must only be placed into slots considered to be low-voltage, isolated, secondary circuits.
- The printed circuit board must be an approved Underwriters Laboratory Inc. component with a flammability rating of UL94 V-1 (minimum) and marked accordingly.
- The printed circuit board must not exceed the specified power available (see Tables 2-10 and 2-11).
- Printed circuit board upgrades must be performed by qualified technical personnel.

Chapter 3

CPU/Motherboard

3.1 Description

The Series 3000 and Series 4000 CPU board is a motherboard design and measures approximately 12 by 14 inches. The board contains the CPU, memory, SIO, timers, memory management, DMA, and calendar logic. Figures 3–1 and 3–2 show the CPU/motherboards in each system unit.

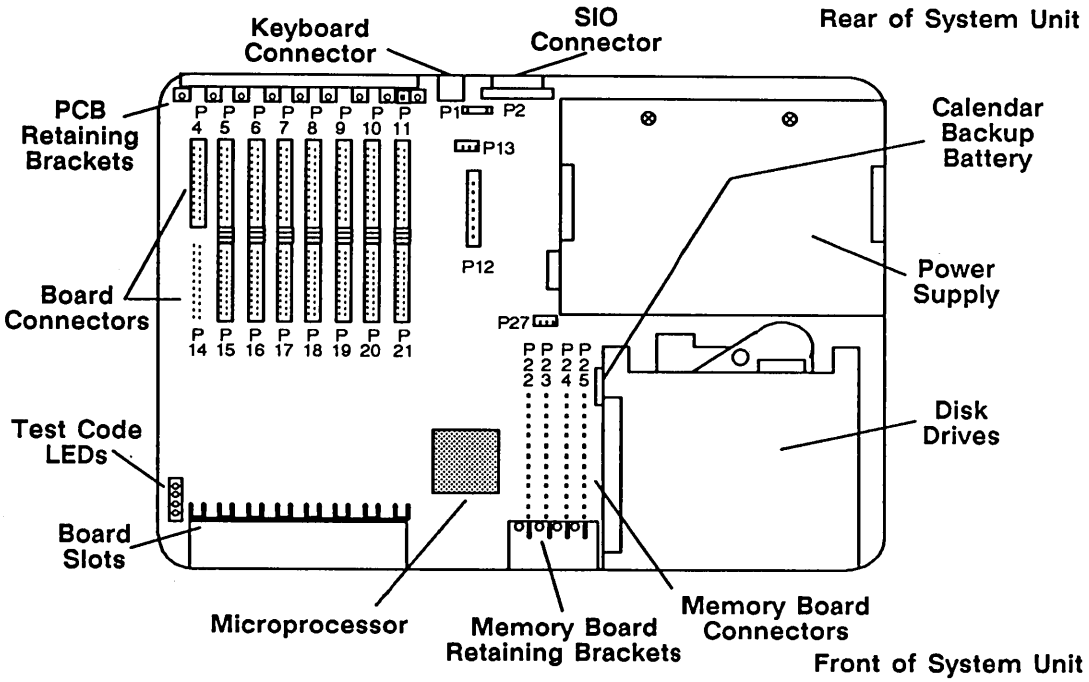


Figure 3–1. Top View of the DS3000 System Unit (With Cover Off)

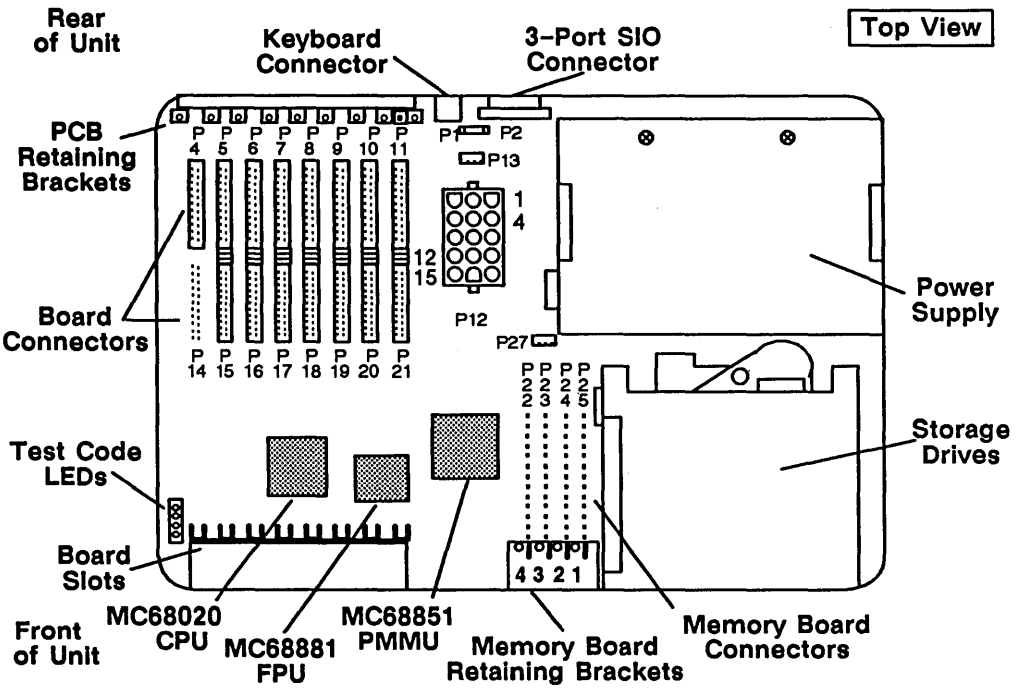


Figure 3–2. Top View of the DS4000 System Unit (With Cover Off)

The following components are used on the CPU/Motherboard:

- Motorola 68020 12–MHz microprocessor in the DS3000, MC68020 25–MHz in the DS4000
- Motorola 68881 floating–point coprocessor daughterboard on the DS3000, on–board chip in DS4000 systems
- Intel 8237A–5 DMA controllers (seven channels)
- Motorola 146818 interval clock and calendar
- Signetics 2681 (DUART) serial port (keyboard)
- One full–duplex progammable serial I/O port in DS3000 systems, three ports in DS4000 systems
- Motorola 6840 interval timer
- Intel 8259A programmable interrupt controller (16 levels of interrupt)
- 32K x 8 EPROM
- Up to 8 MB of CPU memory in DS3000 systems, up to 32 MB in DS4000 systems
- Battery backup for calendar
- Keyboard connection
- Six AT–compatible I/O slots with one 36–pin and one 62–pin card edge connector, seven on newer DS3000 systems and all DS4000 systems (see Chapter 2)
- One XT–compatible I/O slot with a 62–pin card edge connector (two in older DS3000 systems)

3.2 System Bus

The internal bus used on the Series 3000 and Series 4000 CPU/Motherboards is divided into two parts. The logical bus and the physical bus. The logical bus supports the MC68020 CPU and the MC68881 floating–point coprocessor. The bus also supports the coprocessor interface protocol for communication with the floating–point coprocessor and the DMMU/PMMU.

The system bus is organized as follows:

- Logical Address Decode
- Logical Address Bus (LA8 to LA31)
- Data Bus (PDATA0 to PDATA31)
- Interrupt and Vector Generation Circuitry
- Bus Control Signals:
  - Logical Address Strobe (LAS–)
  - Logical Data Strobe (LDS–)
  - Transfer Direction (R/W–)
  - Transfer ACKnowledge (DSACK0 + 1–)
  - Transfer Size (SIZ0 + 1)
- Logical Bus Arbitration:
  - Logical Bus Request (LBR–)
  - Logical Bus Grant (LBG–)
  - Logical Bus Grant ACKnowledge (LBGACK–)
- Halt (HALT–)
- Bus ERRor (BERR–)
- Interrupt Priority Levels (IPL0 – IPL2)
- Function Codes (FC0 – FC2)

The least–significant address bits LA13 through LA19 on the logical bus are used to decode CPU space accesses. The devices selected from this decode are the DMMU in the DS3000, PMMU in the DS4000, the floating–point coprocessor, and the interrupt vector generation circuitry.

The interrupt priority encoding and vector generation are done on the logical bus. When an interrupt is recognized by the CPU, an interrupt acknowledge cycle is performed. This cycle is a CPU space cycle that fetches the vector number of the interrupting device. Interrupt circuitry on the *Domain System* uses two Intel 8259 Interrupt Controllers. Table 2–3 in Chapter 2 shows interrupt level organization.

Address	Device
009400	Interrupt Controller 1
009500	Interrupt Controller 2

Contents of Interrupt Vector Byte

	7	6	5	4	3	2	1	0
IRQ7	T7	T6	T5	T4	T3	1	1	1
IRQ6	T7	T6	T5	T4	T3	1	1	0
IRQ5	T7	T6	T5	T4	T3	1	0	1
IRQ4	T7	T6	T5	T4	T3	1	0	0
IRQ3	T7	T6	T5	T4	T3	0	1	1
IRQ2	T7	T6	T5	T4	T3	0	1	0
IRQ1	T7	T6	T5	T4	T3	0	0	1
IRQ0	T7	T6	T5	T4	T3	0	0	0

The parity error interrupt is a non–maskable interrupt to the CPU. It generates a Level 7 interrupt to the CPU. When the vector is fetched, it comes from the Level 7 autovector location in the CPU exception table (0 x 07c).

There are two sources of this interrupt condition: the RAM parity circuit on the CPU/motherboard, and the devices that generate the IO_CH_CHK.L signal on the I/O bus. The interrupt handler checks the status register to detect which one of these conditions exists. Writing to the status register clears the interrupt status.

The rest of the interrupts are channeled through the interrupt controllers on the CPU board. When the CPU detects an interrupt and an interrupt acknowledge cycle is performed, the interrupt vector offset is fetched from one of the two interrupt controllers. This offset contains the level on the controller IRQ inputs in the three least-significant bits. The remaining bits contain the programmed information.

The physical bus makes the connection through an interface to all of the devices in the *Domain System* such as the DMA channels, serial port, keyboard, calendar, system RAM, system ROM, and all of the devices on the AT-compatible bus. The bus consists of the following signals:

- Physical Address bus (PA0-PA23)
- Physical Data bus (PDATA0-PDATA31)
- Physical Address Strobe (PAS-)
- Physical Data Strobe (PDS-)
- Physical Bus Request (PBR-)
- Physical Bus Grant (PBG-)
- Physical Bus Grant ACKnowledge (PBGACK-)

3.3 Series 3000 and Series 4000 Memory System

The DS3000 CPU supports up to 8 MB RAM. The RAMs used in the DS3000 are 256K x 1 DRAMs with 120 nanoseconds RAS access time and 60 nanoseconds CAS access time. The DS4000 CPU supports up to 32 MB RAM. The RAMs used in the DS4000 are 1 MB x 1 DRAMs with 120 nanoseconds RAS access time and 60 nanoseconds CAS access time.

The memory array consists of 36 RAM chips. Thirty-two of these are used for data. The other four chips are used for the parity circuitry. The support chips for the memory array consist of multiplexers for row and column addresses, circuitry to generate the RAS and CAS clocks for the RAMs, MOS drivers to drive the inputs of the DRAMs, circuitry to decode RAM banks and bytes, and circuitry to generate and check parity of the data in the RAMs.

The RAM refresh is generated by a state sequencer that provides the appropriate timing and signal generation to refresh the on-board RAM and any RAM that may be on the AT-compatible bus. The refresh period is generated by the timer in the SIO DUART (2681) at a period of 15 microseconds.

The refresh interval of DRAMs is 4 milliseconds. This means that all 256 row addresses of DS3000 RAM or all 1000 row addresses of DS4000 RAM must be refreshed in that time.

The parity circuitry for the memory array uses four F280 parity checker/generators to generate the parity bits on Write operations and to check the parity bits on Read operations. The parity circuitry can be forced bad by inputting to the F280 and writing into the parity RAM in diagnostic mode. This approach provides sufficient coverage of the parity circuitry for diagnostics. There is also a 32K x 8 EPROM on the CPU/Motherboard.

3.4 AT-Compatible Bus Interface

One of the features of the *Domain System* is the AT-compatible bus. This feature allows most devices designed to operate on the AT to run on the *Domain System*. The normal AT bus cycle takes 500 nanoseconds for 16-bit transfers. It takes 1 microsecond for 8-bit transfers to 8-bit devices. It takes 2 microseconds for 16-bit transfers to 8-bit devices. These are the minimum cycle times for devices on the AT bus. However, a device may lengthen the cycle by using the IO_CH_RDY signal on the AT bus. In the DS3000 when this signal is negated, the cycle time increases by an integral number of 6-MHz clocks (167 nanoseconds) until it is asserted. In the DS4000 when this signal is negated, the cycle time increases by an integral number of 8-MHz clocks (125 nanoseconds) until it is asserted. Be careful not to assert this signal for more than 2.5 microseconds when using it to extend a cycle.

3.5 Direct Memory Access

The *Domain System* AT-compatible bus uses the Intel 8237 DMA Controller Chip. There are two DMA controllers used on the *Domain System* CPU. One controller supports only 8-bit transfers (Channels 0 through 3), while the other supports 16-bit transfers (Channels 5 through 7). For programming information, see the *Domain Series 3000/Series 4000 Hardware Architecture Handbook* (007861).

The fastest implicitly addressed transfer that can occur takes 1.66 microseconds in the DS3000 and 1.25 microseconds in the DS4000. The CPU supports implicit transfers only. Memory-to-memory transfers may be performed only in the diagnostic mode.

The Intel 8237 DMA Controller has a 16-bit address bus. This means a memory mapper must provide the upper 8 bits of address during a DMA transfer. This device is the 74LS612 Memory Mapper. This device must contain the address of the 64-KB block that the DMA is transferring into memory. Channel 4 is used to cascade Channels 0 through 3 to the CPU.

The two Intel 8237-5 DMA Controllers are concatenated to provide seven usable channels:

Controller 1	Controller 2
CH0 unused	CH4 cascade for Controller 1
CH1 SDLC option	CH5 unused
CH2 floppy	CH6 unused
CH3 unused	CH7 unused

Controller 1 contains Channels 0 through 3, which are used for 8-bit transfers to or from 8-bit devices. Transfers must consist of 64-KB blocks. Controller 2 is used for 16-bit transfers and contains Channels 4 through 7. Channel 4 is used to cascade Channels 0 through 3 from Controller 1 to the processor. Channels 5 through 7 are also on this controller. This controller must not transfer out of 128-KB blocks or on odd-word boundries.

3.6 Calendar

The calendar chip used on the CPU/Motherboard is the MC146818. This device combines three features: a time-of-day clock with an alarm and a 100-year calendar, a programmable periodic interrupt and square-wave generator, and 50 bytes of low-power static RAM. The RAM is used to store configuration information. The calendar chip has a backup battery to ensure that no data is lost when the ac power is removed.

3.7 Diagnostic LED Indicators

The DS3000 has nine LED indicators for diagnostics that can be set or reset by writing to the upper byte of the control register. Four of these LEDs (in one block) are on the CPU/Motherboard to the left of the board slots (looking from the front of the system). The other five LEDs are on the front panel (the green PWR LED is not used for diagnostic error reporting). Figure 3–2 shows the location of these LEDs.

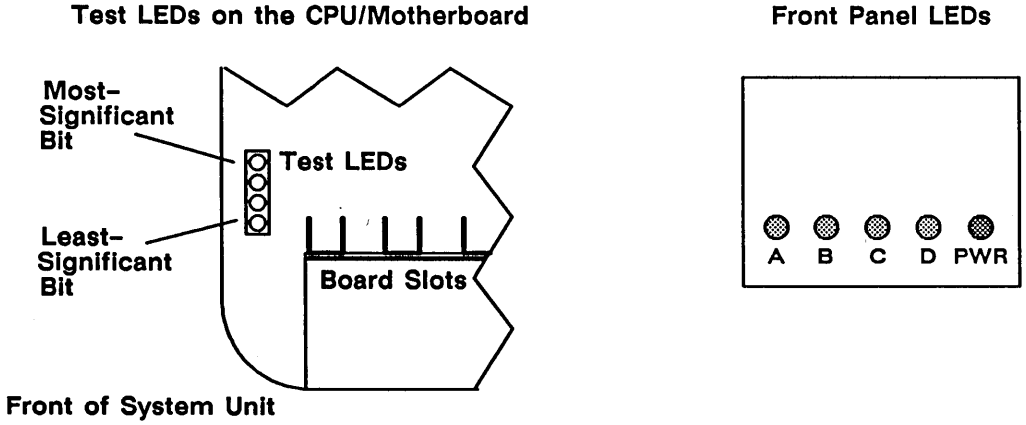


Figure 3–3. Domain System LED Indicator Lights

3.8 Interval Time Clocks (MC6840)

Three 16–bit timing elements are contained within an LSI Timer device. For more detailed information, see Motorola's specification of the MC6840. For programming information, see the *Domain Series 3000/Series 4000 Hardware Architecture Handbook*.

Timer 1

Timer 1's input is a 250–kHz (4–microsecond period) signal.

Timer 2

Timer 2's input is a 125–kHz (8–microsecond period) signal.

Timer 3

Timer 3's input is a 62.5–kHz (16–microsecond period) signal. The Timer 3 input may be prescaled to make the effective input signal have a 128–microsecond period.

3.9 Serial Interface

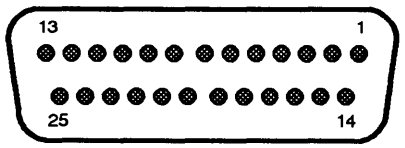
There are two full–duplex serial ports in the DS3000; four in the DS4000. These ports are fully programmable (bit rate, character length, parity, stop bits, etc.).

SIO line 0 interfaces the keyboard to the CPU in the *Domain System*. Port 1 in the DS3000 and ports 1, 2, and 3 in the DS4000 interface serial asynchronous devices to the CPU. All ports are implemented using the Signetics 2681 dual asynchronous control chip. This device has an on–chip baud rate generator, which operates up to 38.4K baud.

As stated, SIO_0 is used for the keyboard and supports full–duplex operation for bidirectional keyboards. The control registers for the keyboard are located at Channel 0 or Channel A.

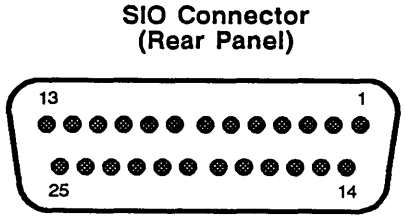
SIO line 1 in the DS3000 and lines 1, 2, and 3 in the DS4000 interface to all other asynchronous devices. The counter/timer on the SIO chip is used for the refresh count. This is set up in the timer mode to produce a square wave output on output OP3. The period of the output is 15 microseconds.

Figures 3–3 and 3–4 show the P2 SIO connector and its pin listings.



Pin #	Signal
1	Ground
2	SIO_TXD
3	SIO_RXD
4	SIO_RTS
5	SIO_CTS
7	In-Line Resistor
8	SIO_DCD
11	SIO_P11
20	SIO_DTR

Figure 3–4. DS3000 P2 SIO Single-Port Connector



Pin #	Signal	Pin #	Signal
1	Ground	16	SIO2_DCD
2	SIO1_TXD	18	SIO2_DTR
3	SIO1_RXD	9	SIO3_RXD
4	SIO1_RTS	10	SIO3_CTS
5	SIO1_CTS	19	SIO3_DTR
7	In-Line Resistor	21	SIO3_TXD
8	SIO1_DCD	23	SIO3_RTS
11	SIO1_P11	25	SIO3_DCD
20	SIO1_DTR	6	Spare
12	SIO2_TXD	17	Spare
13	SIO2_RXD	22	Spare
14	SIO2_RTS	24	Spare
15	SIO2_CTS		

Figure 3–5. DS4000 P2 SIO 3-Port Connector

The interface to SIO line 1 in the DS3000 and SIO1, 2, and 3 in the DS4000 is via RS–232 drivers and receivers. The protocol supports the following signals:

- Serial Transmit Data
- Serial Receive Data
- Data Terminal Ready
- Data Carrier Detect
- Request To Send
- Clear To Send

Chapter 4

Power Supply

This chapter provides the electrical, environmental, and mechanical specifications for the Series 3000 and Series 4000 power supplies (see Figure 4–1). The supplies can be operated either from a 120–V ac or a 220/240–V ac input. Input voltage is selected with switch S2 at the rear of the power supplies.

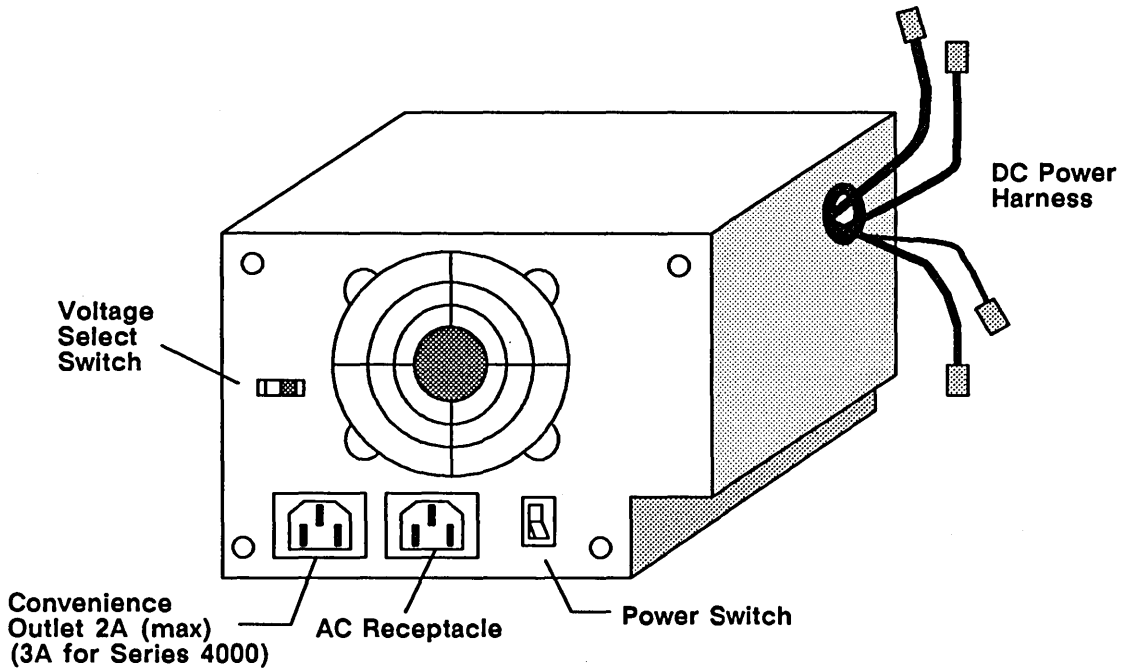


Figure 4–1. Domain System Power Supply

4.1 Electrical Specifications

These specifications apply to the entire power system, including the voltage sources to the option boards.

4.1.1 Output Voltages

Table 4–1 lists the output voltages supplied at the various connector leads in the DS3000 power supply. Table 4–2 lists the output for the DS4000.

Table 4–1. Series 3000 Output Voltages

Voltage (V dc)	Tolerance At Option Board Slot (Volts)	Tolerance At P12 Connector (Volts)	Current (Amps)	P12 Connector Pin No.	Wire Color
+5	4.80 to 5.25	4.85 to 5.26	10 to 24	2, 11, 12, and 13	Red
+12	11.60 to 12.40	11.60 to 12.40	1 to 6	3	Violet
–12	–11.40 to –12.70	–11.35 to –12.65	0 to 0.5	4	Green
–5	–4.70 to –5.75	–4.60 to 5.40	0 to 0.5	9	Yellow
Ground	–	–	–	5, 6, 7, and 8	Black
+8.5	7.70 to 10.75	7.70 to 10.75	N/A	14	Brown
Voltage	**Tolerance**	**Tolerance At P13 Connector**	**Current**	**P13 Connector Pin No.**	**Wire Color**
+7.5	6.65 to 8.35	6.65 to 8.35	N/A	Differential between Pins 1 and 2	Red Black
Voltage	**Tolerance**	**Tolerance At P10 or P11 Connector**	**Current**	**P10 or P11 Connector**	**Wire Color**
+5	4.85 to 5.25	4.85 to 5.25	N/A	4	Red
+12	11.60 to 12.40	11.60 to 14.40	N/A	1	Violet
Ground	–	–	–	2 and 3	Black

This includes all line loads and temperature ranges. The Series 3000 power supply also provides 120 V ac at 0 to 2 A rms and 220 V ac at 0 to 1 A rms to the convenience outlet.

Table 4–2. Series 4000 Output Voltages

Voltage (V dc)	Tolerance At Option Board Slot (Volts)	Tolerance At P12 Connector (Volts)	Current (Amps)	P12 Connector Pin No.	Wire Color
+5	4.80 to 5.25	4.95 to 5.26	10 to 40	2, 4, 5, 6, 7	Red
+12	11.60 to 12.40	11.60 to 12.40	0.1 to 0.5	14 (3A limited)	White
–12	–11.25 to –12.80	–11.25 to –12.75	0 to 0.75	3	Green
–5	–4.60 to –5.75	–4.60 to –5.40	0 to 0.75	1	Yellow
Ground	–	–	–	8, 9, 10, 11, 12	Black
+12	11.60 to 12.40	11.60 to 12.40	1 to 2	15	Violet
Voltage	**Tolerance**	**Tolerance At P13 Connector**	**Current**	**P13 Connector Pin No.**	**Wire Color**
+12	–	11.60 to 12.40	0.50	Differential between Pins 1 and 2	Red Black
Voltage	**Tolerance**	**Tolerance At P10 or P11 Connector**	**Current**	**P10 or P11 Connector**	**Wire Color**
+5	–	4.95 to 5.30	0 to 2	4	Red
+12	–	11.60 to 12.40	1 to 4	1	Violet
Ground	–	–	–	2 and 3	Black

This includes all line loads and temperature ranges. The Series 4000 power supply also provides 120 V ac at 0 to 3 A rms and 220 V ac at 0 to 1.5 A rms to the convenience outlet.

4.1.2 Operating Parameters

Table 4-3 lists the power supply's operating parameters.

Table 4-3. Power Supply Operating Parameters

Parameters	Conditions	Specifications	
		DS3000	DS4000
Input Voltage	All rated load conditions	90 to 132 V ac rms 187 to 264 V ac rms	90 to 132 V ac rms 187 to 264 V ac rms
Nominal Line	120/240 V ac	Switch Selectable	Switch Selectable
Input Frequency	-	50 Hz (± 3 Hz) 60 Hz (± 3 Hz)	50 Hz (± 3 Hz) 60 Hz (± 3 Hz)
Overvoltage Protection	+5 V and -5 V dc +12 V and -12 V dc	6.25 V (± .75 V) 14 V (+2.0 V, -1.0 V)	6.25 V (± .75 V) 14 V (± 1.0 V)
Output Power		210 Watts	288 Watts
AC Leakage Current to GND*	Input 250 V ac rms 50 Hz	2.5 mA maximum	2.5 mA maximum
Ripple and Noise ** (peak-to-peak)	All outputs within line and load specifications (500 KHz bandwidth)	+5 V (2%), +12 V (1%) -5 V and -12 V (2.5%)	+5 V (2%), +12 V (1%) -5 V and -12 V (2.5%)
Load Current	+5 V dc -5 V dc +12 V dc -12 V dc 120 V ac 240 V ac	10 A minimum, 24 A maximum 0 to 0.5 A 1 A minimum, 6 A minimum 7.4 A peak for 20 seconds 0 to 0.5 A 0 to 2 A rms 0 to 1 A rms	10 A minimum, 40 A maximum 0 to 0.75 A 1 A minimum, 6 A minimum 7.4 A peak for 20 seconds 0 to .75 A 0 to 3 A rms 0 to 1.5 A rms
AC Input Current	90 to 132 V rms 187 to 264 V rms	7.4 A rms * * * 3.7 A rms * * *	11 A rms * * * 5.5 A rms * * *
Hold Up Time	After the POWER GOOD signal goes low (false), the supply voltages hold within tolerance for 500 µsec (2 msec for Series 4000). (See Figure 4-2.)		

* Not including monitor leakage current.

* * Radio frequencies are involved when measuring ripple and noise. Spurious pickup is a constant possibility. To minimize these problems, you should measure noise and ripple using a 1:1 probe with the shortest possible lead length outside the grounded cable.

* * * Includes convenience load.

NOTICE: The power supply has an input (J100) and an output (P100) ac connector. The P100 connector should be used to supply power to a monitor. The combined leakage of the supply and the display current should be less than 3.5 mA for all input requirements.

Figure 4–2 shows the timing after the POWER GOOD signal goes low (false). Note that the supply voltages hold within tolerance for 500 microseconds for the Series 3000, and 2 milliseconds for the Series 4000.

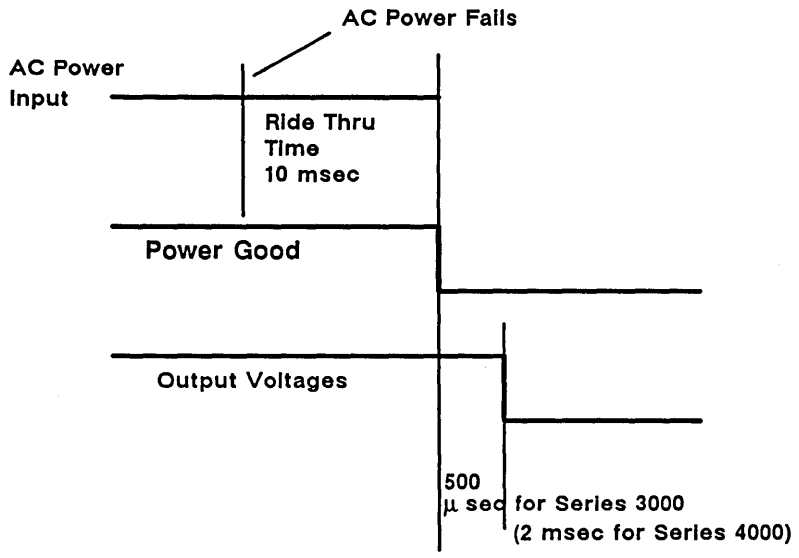


Figure 4–2. Hold Up Time

4.1.3 Power Supply Connectors

The power supply has two ac connectors. J100 is the input power connector (Power Dynamics part number 42R02–4212 or equivalent). P100 is the output power connector (Power Dynamics number 43R03–1121 or equivalent). It should be used as the power source for the monitor.

Power supply dc voltages are distributed to the system via the P10, P11, P12, and P13 connectors.

4.1.3.1 P10 and P11 – Disk Subsystem Power Connectors

P10 and P11 are 4–pin connectors that are identical and interchangeable. They carry power to the disk and diskette subsystem. P10 and P11 are AMP connectors (part number 1–480424–0, with part number 60619–4 contacts or equivalent).

4.1.3.2 P12 – System Power Connector

In the Series 3000, P12 is a 14–pin connector that carries power to the printed circuit boards. P12 is a Molex connector (part number 26–03–4141). The contacts are part number 08–50–0189 (or equivalent) and the polarizing key is part number 89–00–3001 (or equivalent). Pin 10 on this connector is a polarizing pin.

In the Series 4000, P12 is a 15–pin connector that carries power to the printed circuit boards. P12 is a Universal 15–pin Mate–N–Lok connector (AMP plug ass'y 350736–1, AMP socket ass'y 350550–3).

4.1.3.3 P13 – System Chassis Fan Power Connector

P13 is a 2–pin connector that carries power to the system chassis fan only. It should not be used for any other system application. P13 is an AMP connector (part number 350777–1 or equivalent). The sockets are part number 350689–1 (or equivalent).

NOTICE: The fan voltage is measured differentially between Pin 1 and Pin 2.

Figure 4–3 shows the destination for the dc connectors in the Series 3000.

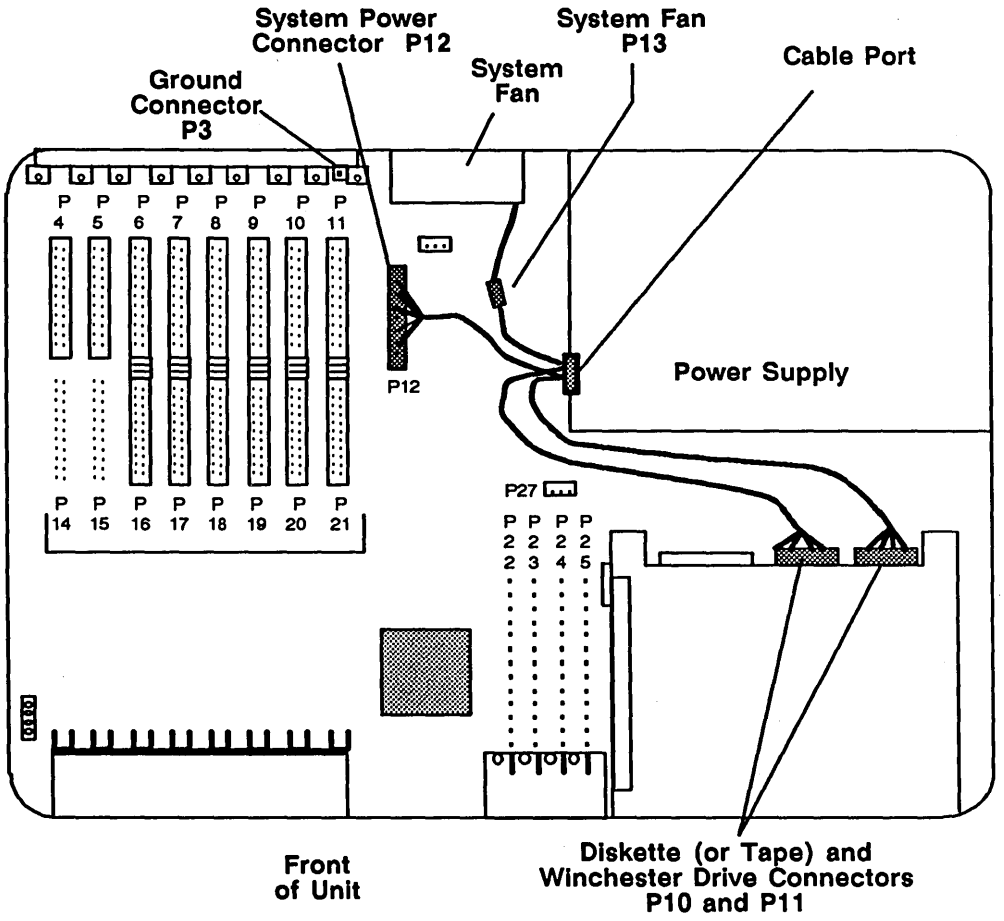


Figure 4–3. Series 3000 DC Connectors Destination

Figure 4–4 shows the destination for the dc connectors in the Series 4000.

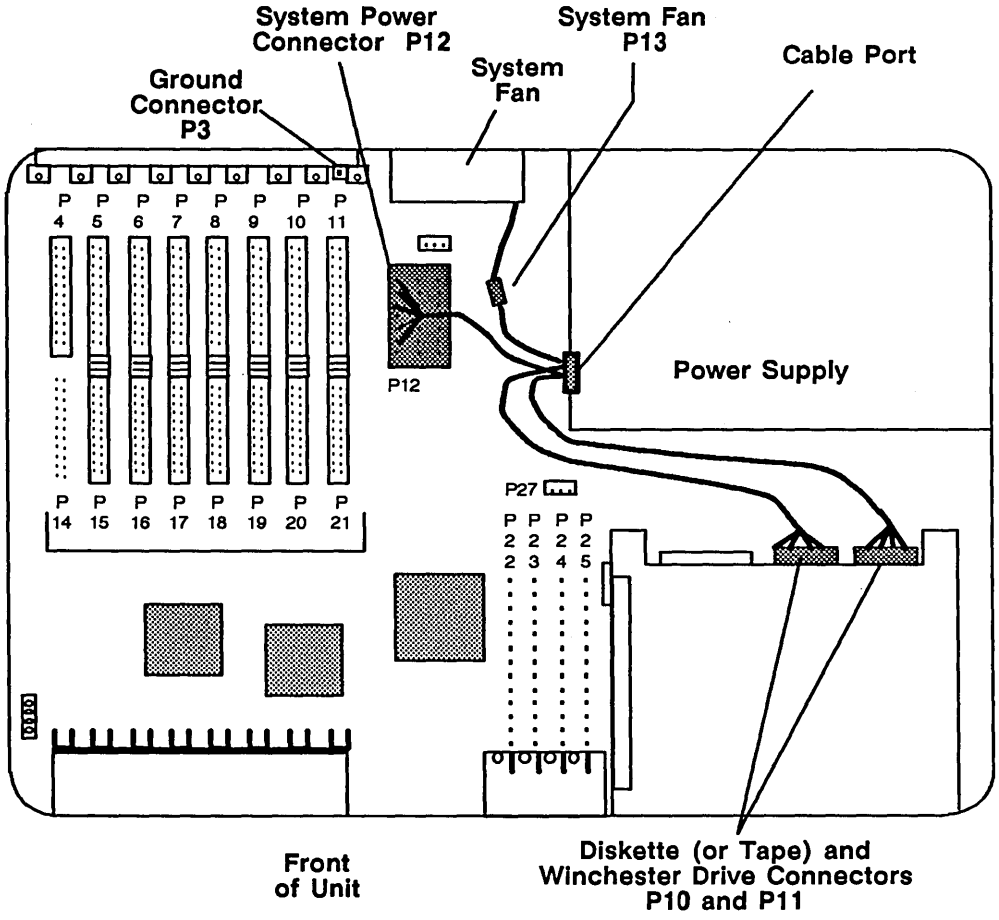


Figure 4–4. Series 4000 DC Connectors Destination

4.1.4 Power Supply and System Protection

In the Series 3000, the power supply is protected by a 6–A fuse. The ac output line is filtered by the input filter and is protected by a fuse within the display monitor (see Figure 4–5). The output line is switched to 120 V or 240 V operation along with the input line. The monitor should be switched to the correct operating voltage in conjunction with the system power supply. The Series 3000 keyboard may be fused with a 3–A, inline, NB fuse at pin 14 of the P12 power conector.

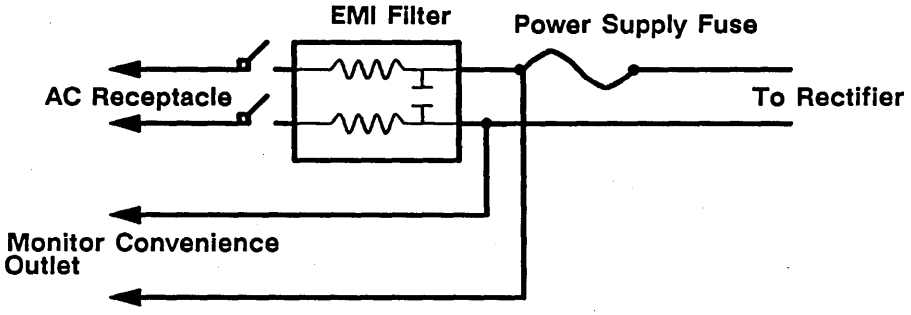


Figure 4–5. Series 3000 AC Lines Protection

In the Series 4000, the power supply is protected by a 10–A fuse. The ac output line is filtered by the input filter and is protected by a fuse within the display monitor (see Figure 4–6). The output line is switched to 120 V or 240 V operation along with the input line. The monitor should be switched to the correct operating voltage in conjunction with the system power supply. The Series 4000 keyboard is fused with a 3–A, inline, NB fuse at pin 14 of the P12 power conector.

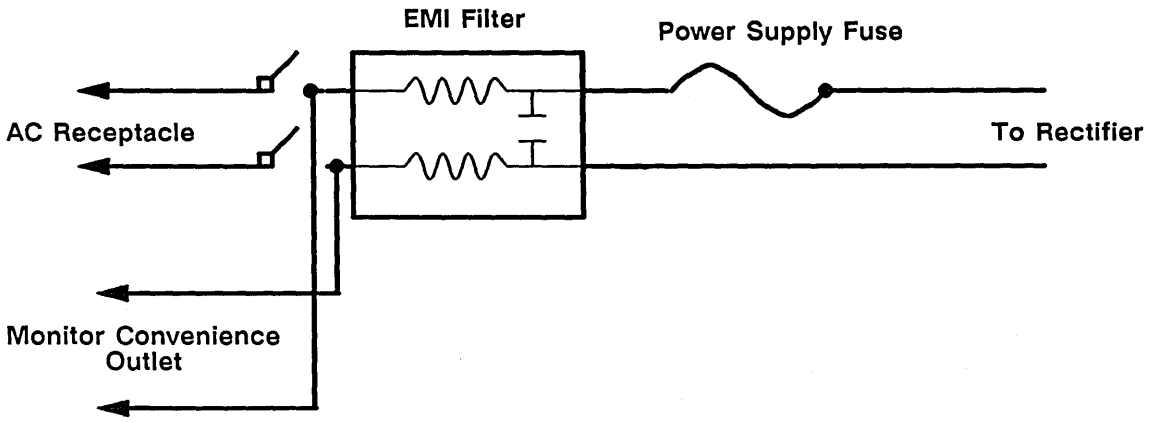


Figure 4–6. Series 4000 AC Lines Protection

When the POWER GOOD signal is asserted (high), it indicates proper power supply operation. When the power supply is turned off for at least 1 second and then turned on, the POWER GOOD signal comes on, if there are no power supply problems. The signal is a logical AND of the dc output sense signals and the ac sense signal. When a power failure is detected in the Series 3000, the AC FAIL Signal forces POWER GOOD low at least 500 µsec before any output voltage falls below regulation limits. When a power failure is detected in the Series 4000, the AC FAIL Signal forces POWER GOOD low at least 2 msec before any output voltage falls below regulation limits.

When both Winchester and tape cartridge drives are present in a system, an inline filter is used on the Winchester drive power supply input. This filter guards against power surges and spikes from the tape drive.

4.2 Environmental Specifications

A fan operating at fixed speed (7.5 V dc for Series 3000, 12 V dc for Series 4000) is mounted on the power supply cage. Air is exhausted from the power supply through the fan. (A similar fan running from the same 7.5 V dc supply in the Series 3000, or 12 V dc in the Series 4000, removes hot air from the system chassis.)

The operating temperature range for the power supply is 15 to 45 degrees C (59 to 113 degrees F) in an ambient operating environment with forced air and the fan running at 7.5 V dc in the Series 3000, or 12 V dc in the Series 4000.

A thermal switch shuts off the dc outputs of the power supply in the event of a power supply thermal overload.

4.3 Mechanical Parameters

Figure 4–7 gives the physical dimensions of the power supplies. The power supplies are located in the upper right–hand corner of the system chassis when looking at the system from the front.

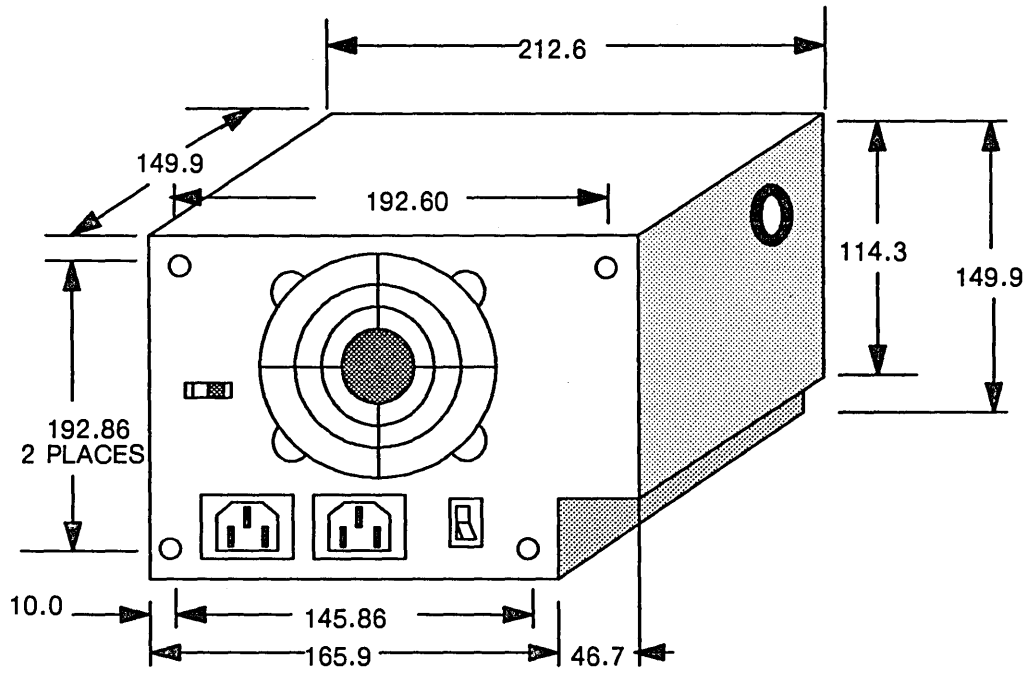


Figure 4–7. Power Supply Physical Dimensions (Centimeters)

In the *Domain System*, the power supply is held in place by four screws at the rear of the system chassis (see Figure 4–8), and by two clips under the power supply case that slip into two tabs in the system chassis.

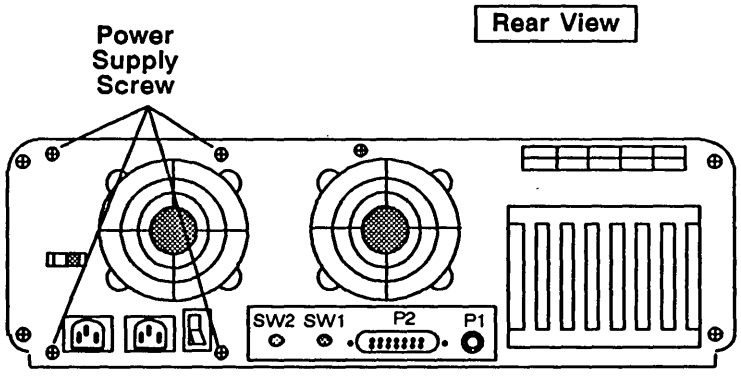


Figure 4–8. Power Supply Mounting

Chapter 5

Winchester/Floppy Disk Controller

This chapter describes the Series 3000 and Series 4000 disk controllers and their operation. Figure 5–1 shows the Winchester/floppy disk controller that is supplied in the DS3000 system unit when it is configured with the 72–MB Winchester disk drive. Several connector and jumper block locations are labeled for later reference. The 72–MB Winchester disk drive uses the OMTI 8800 disk controller.

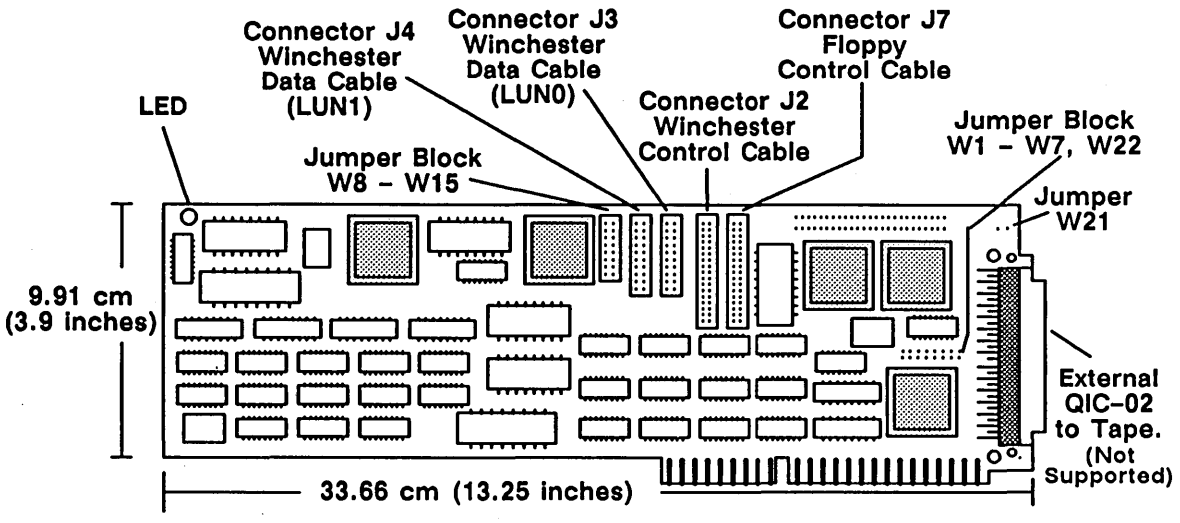


Figure 5–1. 8800 Disk Controller Board Component Locations

Figure 5–2 shows the OMTI 8610 Winchester/floppy disk controller that is supplied in the DS3000 system unit when it is configured with either the 72–MB, 155–MB or 348–MB Winchester disk drive. Several connector and jumper block locations are labeled for later reference. The 348–MB drive will only operate with Revision C or later versions of this controller.

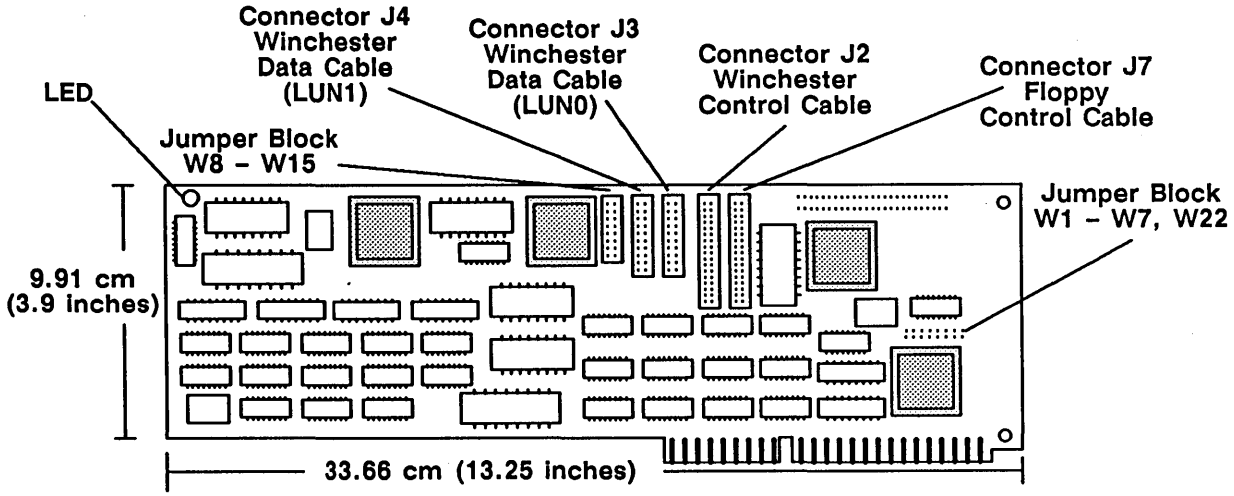


Figure 5–2. 8610 Disk Controller Board Component Locations

Figure 5–3 shows the OMTI 8621 Winchester/floppy disk controller that is supplied in the DS3000 and DS4000 system units when they are configured with the 155–MB or 348–MB Winchester disk drive. Several connector and jumper block locations are labeled for later reference. This is the only Winchester/floppy disk controller supplied with the DS4000.

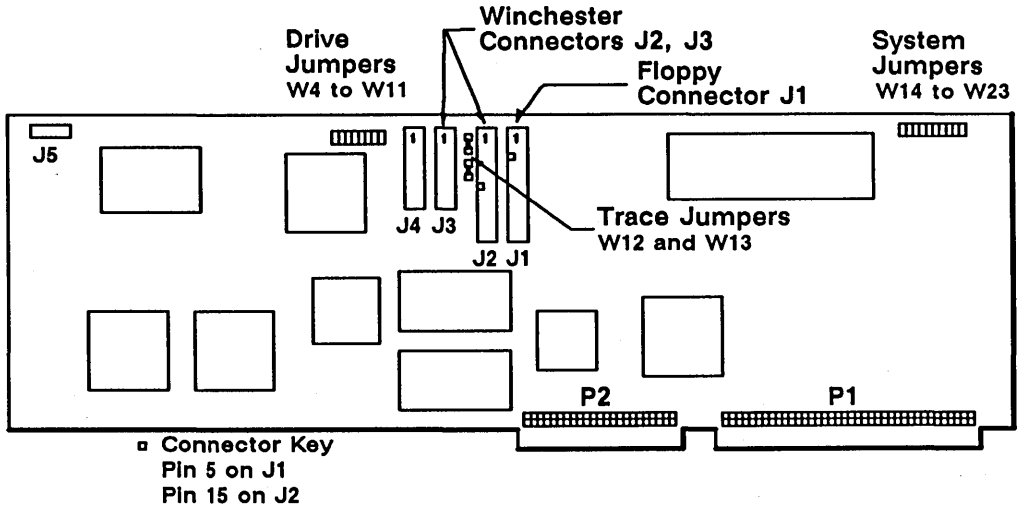


Figure 5–3. 8621 Disk Controller Board Component Locations

5.1 Introduction

The disk controllers have the following features when used in a *Domain System*:

- Operate one or two ST506/412 Winchester disk drives (the 8610 and 8621 operate the 155-MB and 348-MB ESDI drives)
- Track address capability up to 2048 tracks
- Automatic write precompensation
- 256-, 512-, 1024-, or 1056-byte sector size for hard disk
- 512- or 1024-byte sector size for floppy disk
- 1:1 interleave for hard disk
- Multiple sector transfer
- Implied, overlapped, and buffered seek capability
- Programmable sector interleaving
- Capable of reading 48- or 96-TPI, IBM-compatible floppy disk
- Capable of writing a 96-TPI floppy disk
- 8-KB data buffer (the 8610 controller has a 32-KB data buffer)
- Less than 10 watts power consumption
- ECC error correction by host or disk controller
- Concurrent data operations on one diskette and one fixed disk drive
- Capable of operating one or two dual-speed floppy disk drives

The disk controller can run up to two ST506/412 interface Winchester disk drives and up to two SA450 interface floppy disk drives (the 8610 controller operates ESDI drives). The *Domain System*, however, only utilizes one Winchester disk and one floppy disk drive in the system unit cabinet.

5.2 Relevant Documentation

The *OMTI 8800 Reference Manual* (OMTI no. 3001241), the *8610 Reference Manual*, and *IBM PC/AT Intelligent Data Controllers Reference Manual* (OMTI no. 3001483) may also be useful.

5.3 Physical Board Specifications

Subsections 5.3.1 through 5.3.5 describe the specifications for the disk controller boards.

5.3.1 Physical Dimensions

- Width 9.91 cm (3.9 inches)
- Length 33.66 cm (13.25 inches)
- Height 1.91 cm (0.75 inches)

The controller occupies one AT-compatible board slot in the system unit (see Chapter 2).

5.3.2 Environmental Specifications

Table 5–1 lists the environmental specifications for the Winchester/floppy disk controller.

Table 5–1. Winchester/Floppy Disk Controller Environmental Specifications

Parameter	Operating	Storage
Temperature	0°C to 50°C	–40°C to 75°C
Relative Humidity	10% to 95%	Noncondensing
Maximum Wet Bulb	30°C	Noncondensing
Altitude	0 to 10000 ft.	0 to 15000 ft.

5.3.3 Power Requirements

- Voltage +5 V (± 5%)
- Maximum ripple and noise (P/P) 100 mV.
- Maximum current drawn 1.3 amps (8621 draw is 1.0 A max.)

5.3.4 Winchester Interface Signals

This subsection defines the signals on the connectors that are the physical interface between the disk controller and the Winchester disk drive.

5.3.4.1 Control Signal Connector

The 34-pin connector on the disk controller boards is labeled **J2**. Table 5–2 lists the control signals carried over connector J2.

Table 5–2. Connector J2 Pin Listing

Ground Pins	Signal Pins	Signals
1	2	Head Select 3/WSI
3	4	Head Select 2
5 *	6	Write Gate
7	8	Seek Complete
9	10	Track 000
11	12	Write Fault
13	14	Head Select 0
15	16	Reserved
17	18	Head Select 1
19	20	Index
21	22	Ready
23	24	Step
25	26	Drive Select 1
27	28	Drive Select 2
29	30	Drive Select 3
31	32	Drive Select 4
33	34	Direction Select

* Pin 5 is keyed for polarity.

5.3.4.2 Data Signal Connectors

The 20-pin data signal connectors are labeled **J3** and **J4** on the disk controller board. Connectors J3 and J4 are for disks using the 506/412 interface standards. J3 is used for LUN0 and J4 is used for LUN1 (to operate a second drive). Table 5-3 lists the signals carried over connectors J3 and J4 of the Winchester/floppy disk controllers.

Table 5-3. Connector J3 and J4 Pin Listings

Pins	506/412 Disks (J3 and J4)
1	Drive Selected
2	Ground
3	Reserved
4	Ground
5	Reserved
6	Ground
7	Reserved
8	Ground
9	Reserved
10	Reserved
11	Ground
12	Ground
13	+MFM Write Data
14	-MFM Write Data
15	Ground
16	Ground
17	+MFM Read Data
18	-MFM Read Data
19	Ground
20	Ground

5.3.5 Floppy Disk Interface Signals

This subsection defines the signals on the connectors that are the physical interface between the disk controller and the floppy disk drive.

Control Signal Connector

The 34-pin (2 by 17 Berg-type) control signal connector is labeled **J7** on the disk controller board. Table 5-4 lists the control signals carried over connector J7.

Table 5-4. Connector J7 Pin Listing

Ground Pins	Signal Pins	Signals
1	2	Density and Speed Control
3	4	Drive Dependent
5 *	6	Drive Dependent
7	8	Index
9	10	Motor On – 1
11	12	Drive Select 2
13	14	Drive Select 1
15	16	Motor On – 2
17	18	Direction Select
19	20	Step
21	22	Write Data
23	24	Write Gate
25	26	Track 00
27	28	Write Protect
29	30	Read Data
31	32	Side 1 Select
33	34	Diskette Change or Ready
*Pin 5 is reserved to polarize the connector.		

5.4 Hardware Description

Subsections 5.4.1 through 5.4.5 contain descriptions of the major components on the disk controller board.

5.4.1 Theory of Operation

The *Domain System* disk controllers are divided into two distinct sections — the floppy disk logic and the Winchester disk logic. These two sections share the same physical PCB, but are otherwise independent. This allows full concurrent operations between the two sections. For example, a DMA data transfer to the floppy could happen at the same time a programmed I/O data transfer occurs on the Winchester disk.

5.4.1.1 Microprocessor

The microprocesssor used on the disk controller board is a Z8681 with an average instruction time of 1.5 microseconds and a maximum instruction time of 3 microseconds. The Z8681 incorporates the following features:

- Full Duplex UART and two programmable 8-bit counter/timers
- 24 I/O lines
- Up to 64-KB addressable external space
- 143-byte register file, including 124 general-purpose registers, four I/O port registers, and 16 Status and Control registers
- Vectored priority interrupts for I/O, counter timers, and UART
- On-chip oscillator that accepts crystal or external clock drive
- Interrupt response time of 26 microseconds

5.4.1.2 Hard Disk Control

The hard disk control hardware uses five VLSI chips from OMTI. These are the OMTI 5060 4-channel DMA Controller, OMTI 5050 disk sequencer controller, OMTI 5080 disk interface controller, OMTI 5090 host interface controller chip, and OMTI 5070 ENDEC control chip. These five VLSI chips, together with a Z8681 microprocessor and local memory, control one or two ST506/412 type hard disks.

5.4.1.3 Floppy Disk Control

The floppy disk control uses two VSLI ICs. These are the FDC765 floppy control chip and the SMC 9229 data separator. All the hardware for the floppy control is independent of the Z8681 microprocessor and is operated entirely by the host CPU. The floppy disk operates using a DMA channel to transfer data.

5.4.2 Host Bus Interface

The host bus interface is AT-compatible (both electrically and mechanically). For more information, refer to Chapter 2 in this document.

Data may be transferred to and from the host CPU in either a byte or word format. The Winchester disk uses the 16-bit (word) data transfer format; the floppy disk uses the 8-bit (byte) data transfer format.

Figure 5-4 shows the byte alignments for both word and byte data transfers.

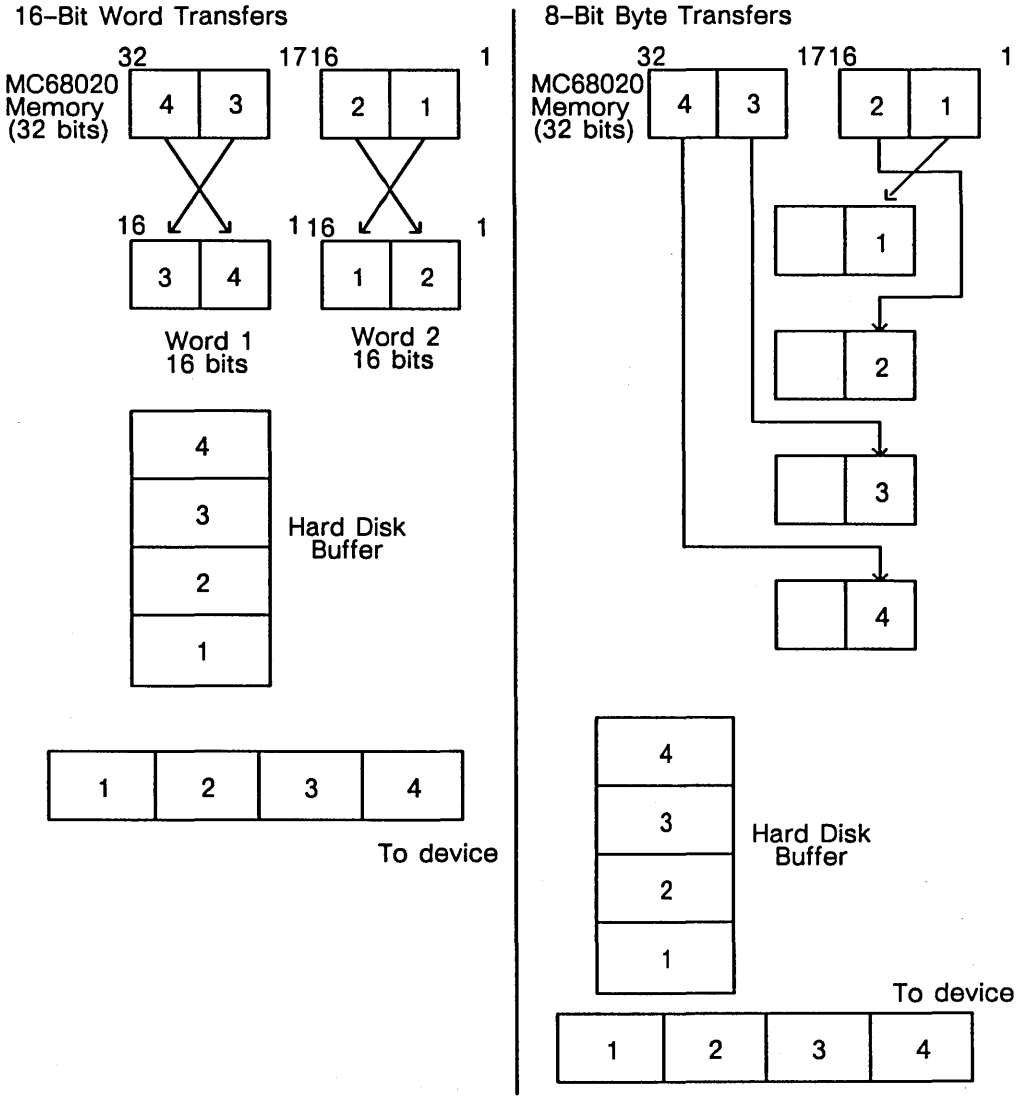


Figure 5-4. Data Transfer Byte Alignments

5.4.3 Jumper Settings

Jumpers are labeled starting with the letter W. Table 5–5 lists the standard jumper settings on the disk controller boards used in the DS3000 and DS4000 system units.

Table 5–5. Disk Controller Jumper Listing

Winchester Disk Drive Used	Jumper Configurations
Micropolis 1325 72-MB * * (8800, 8610, or 8621 Controller0	**W1** W2 W3 **W4** W5 W6 **W7** **W22** * **W8** **W9** W10 W11 W12 W13 W14 W15
Micropolis 1355 155-MB (8610 or Controller)	W1 W2 W3 **W4** W5 W6 **W7** W22 **W8** **W9** W10 **W11** W12 W13 W14 W15
Maxtor EXT-4380 348-MB (8610, Rev. C and later)	**W1** **W2** W3 **W4** W5 W6 **W7** W22 **W8** **W9** W10 **W11** W12 W13 W14 W15
Micropolis 1355 155-MB (OMTI 8621 Controller)	**W16** **W17** W18 W19 **W20** W21 W22 W23 W7 **W8** W9 **W10** **W11** **W13** W14 W15
Maxtor EXT-4380 348-MB (OMTI 8621 Controller)	**W16** **W17** W18 W19 **W20** W21 **W22** **W23** W7 **W8** W9 **W10** **W11** **W13** W14 W15

BOLDFACE Indicates Jumper **IN**

The controller operates properly with W21 IN or OUT.
* W22 must be In on Rev. C or Lower.
* * DS3000 only

5.4.4 Controller Initialization

At power-on or any reset operation, the controller will light the red LED at the top left of the board and proceed to perform the controller diagnostics. These are the same diagnostics performed when (if) software issues a controller diagnostic command (hex E4). If one of the diagnostics fails, then the red LED will remain ON. It is not possible to issue a disk-related command to the controller board without having it rejected. It is possible, if the LED remains ON, to issue one of the diagnostic commands and to then check the sense bytes to determine which of the diagnostics failed. If all of the diagnostics pass, then the red LED is turned off and disk-related commands can be issued to the controller.

5.4.5 Winchester Disk Drive Initialization

At power-on or any reset operation, the controller defaults to the following parameters for Winchester disks. The hex values refer to the parameter list of the Initialize command.

NUMBER OF HEADS = 4	(hex 03)
MAXIMUM CYLINDER ADDRESS (Most-Significant Bit) = N/A	(hex 01)
MAXIMUM CYLINDER ADDRESS (Least-Significant Bit) = 306	(hex 31)
REDUCED WRITE CURRENT = 153	(hex 80)
WRITE PRECOMPENSATION CYLINDER = 153	(hex 80)

Chapter 6

Winchester Disk Drive

6.1 Scope

The Winchester disk drives used in the Series 3000 and Series 4000 have unformatted capacities of 85-MB (DS3000 only), 170-MB, and 380-MB, respectively. These drives have a formatted capacity of 72-MB (DS3000 only), 155-MB, and 348-MB. Throughout this chapter we will refer to the formatted (usable) capacity of the drive.

This chapter lists the requirements for the 5 1/4-inch, 72-MB (ST412 interface), 155-MB, and 348-MB (ESDI interface) Winchester disk drives. Figure 6-1 is a front view of the system unit with the top cover removed to show the location of the Winchester disk drive.

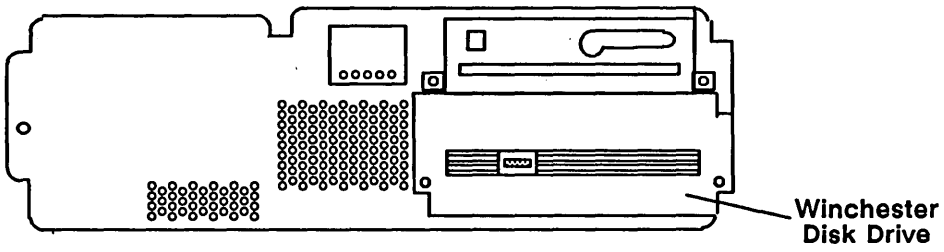


Figure 6-1. Front View of the System Unit

6.2 Required Design Features

The DS3000 and DS4000 Winchester disk drives must meet the following specifications:

- They must have a form factor and mounting holes that are compatible with the industry standard for full-height, 5 1/4-inch, rigid disk drives (that is, Seagate ST506).
- The 72-MB drive must have a buffered seek mode that is compatible with a 6-microsecond step pulse rate. (This drive is used in the DS3000 only.)
  The 155-MB and 348-MB drives must operate in the serial mode.
- The 72-MB drive must not require the host controller to perform write current reduction operations (DS3000 only).
- The drives must use only +5 V dc and +12 V dc power, with no power sequencing required.
- The drives must conform to the power supply specifications in Tables 6-10 and 6-11.
- The drives must automatically move the recording heads to a landing zone (completely free of user data) and latch them there upon the loss of dc power.
- The drives must provide an automatic brake to decelerate the disks when power is removed.
- The 72-MB drive must not indicate a fault if a seek to a cylinder greater than the maximum cylinder is requested (DS3000 only).
- The 72-MB drive must have a minimum unformatted capacity of 85-MB.
  The 155-MB drive must have a minimum unformatted capacity of 170-MB.
  The 348-MB drive must have a minimum unformatted capacity of 380-MB.
- The 72-MB drive must be interface-compatible with the Seagate ST412 disk drive at a data transfer rate of 5.0 megabits/second (MFM) (DS3000 only).
  The 155-MB and 348-MB drives must be interface-compatible with ESDI disk drives at a data transfer rate of 10.0 megabits/second (NRZ).
- The 72-MB drive must be formattable for 9 sectors per track (1114 total bytes in each sector).
  The 155-MB and 348-MB drives must be formattable for 18 sectors per track (1056 total bytes in each sector).

6.3 Interface Specifications

The 72-MB drive, used only in the DS3000, should be functionally and electrically compatible with the industry-standard ST412 rigid disk drive interface, transferring MFM data at 5.0 megabits/second. The 155-MB and 348-MB drives should be functionally and electrically compatible with the industry-standard ESDI rigid disk drive interfaces, transferring NRZ data at 10.0 megabits/second.

The control signals on J1 and the nondifferential signals on J2 terminate with 220 ohms (± 5%) to +5 V, and 330 ohms (± 5%) to ground at the last receiver on the cable.

The differential data signals on J2 terminate with 100 ohms (± 5%) between the + and – signals of each pair at each receiver.

The terminating resistors for the control signals are housed in a removable terminator pack supplied with each drive. The terminating resistors for the data signals are permanently installed in each drive.

The control signal cable (part number 004006-034) can be daisy-chained to a maximum cable length of 10 feet (3.0 meters). The data signal cable (part number 004006-020) is radial, with a maximum length of 10 feet (3.0 meters).

The control and data cables are 3M Scotchflex #3365/34 and #3365/20 flat ribbon cables, respectively (or the equivalent). The mating cable connectors are (3M Scotchflex) as follows:

P1: 003997-034 (3M #3463-0001; key between pins 4 and 6)
P2: 003997-020 (3M #3461-0001; key between pins 4 and 6)

Tables 6-1 and 6-2 list the pin assignments for the control signal connector J1 and the data signal connector J2.

NOTICE: The dash (-) symbol following any signal in the following tables indicates that the signal is low true.

Table 6-1. Control Signal Connector J1 Pin Assignments

J1 Connector Pin			
Signal	Ground	Signal Name	Source
2	1	HEAD SELECT 2 (to the third-)	Host
4	3	HEAD SELECT 2 (to the second-)	Host
6	5	WRITE GATE-	Host
8	7	SEEK COMPLETE-	Drive
10	9	TRACK 0-	Drive
12	11	WRITE FAULT-	Drive
14	13	HEAD SELECT 2 (to the 0-)	Host
16	15	Reserved (to J2 Pin 7)	-
18	17	HEAD SELECT 2 (to the first-)	Host
20	19	INDEX-	Drive
22	21	READY-	Drive
24	23	STEP-	Host
26	25	DRIVE SELECT 1-	Host
28	27	DRIVE SELECT 2-	Host
30	29	DRIVE SELECT 3-	Host
32	31	DRIVE SELECT 4-	Host
34	33	DIRECTION IN-	Host

Table 6-2. Drive Data Signal Connector J2 Pin Assignments

J2 Connector Pin			
Signal	Ground	Signal Name	Source
1	2	DRIVE SELECTED-	Drive
3	4	Reserved	-
5	6	Reserved	-
7	8	Reserved (to J1 Pin 16)	-
9	10	Reserved	-
-	11	Ground	-
-	12	Ground	-
13	-	MFM WRITE DATA+	Host
14	-	MFM WRITE DATA-	Host
-	15	Ground	-
-	16	Ground	-
17	-	MFM READ DATA+	Drive
18	-	MFM READ DATA-	Drive
-	19	Ground	-
-	20	Ground	-

Figure 6–2 shows the ribbon cable connections to the Winchester disk drive and disk controller.

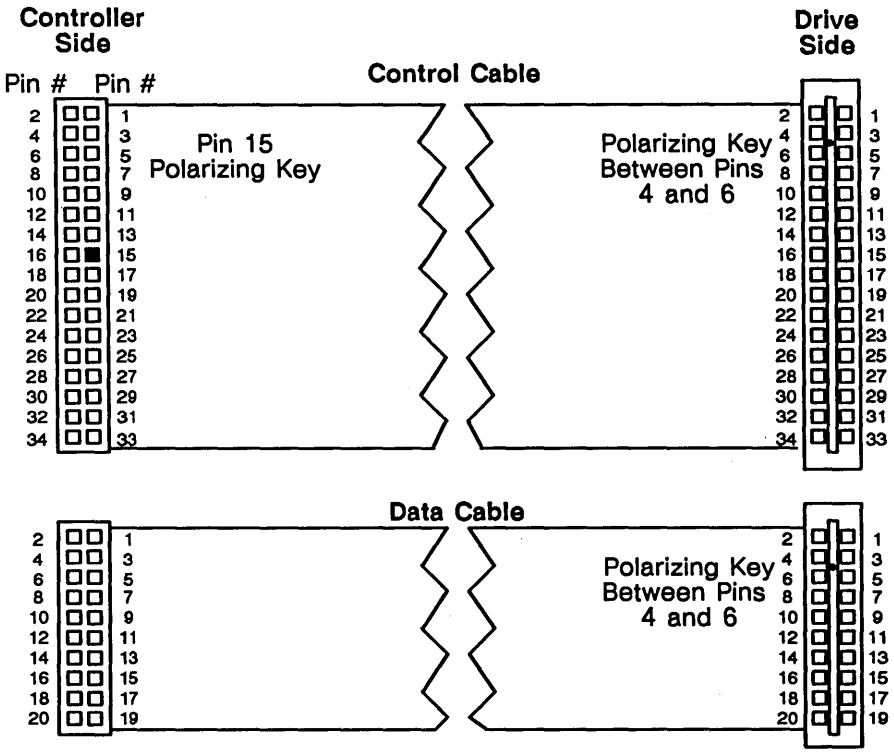


Figure 6–2. Winchester Disk Drive Ribbon Cable Connectors

Figure 6–3 shows the P10 connector from the power supply and lists the voltages supplied to the Winchester disk drive.

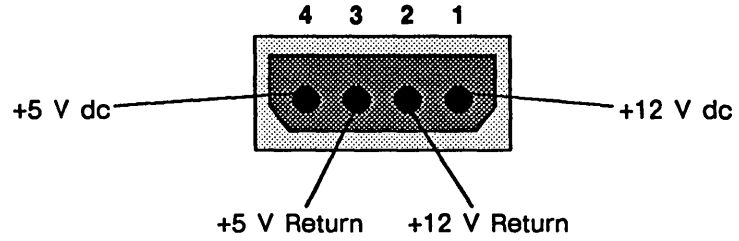


Figure 6–3. P10 Winchester Drive Power Supply Input Connector

6.4 Performance Specifications

Tables 6–3, 6–4, and 6–5 list the operating characteristics of the approved Winchester disk drives.

Table 6–3. Approved 72–MB Winchester Disk Drive Specifications (DS3000 only)

Operating Characteristics (Unformatted)	Micropolis 1325
Transfer rate (MB/second)	5
Track–to–track seek time (typical)	6 msec
Average seek time (typical)	28 msec
Maximum seek time (typical)	62 msec
Average latency	8.33 msec
Bytes per track	10,416
Tracks per inch	N/A
Bits per inch	N/A
Number of data surfaces	8
Nominal rpm	3600

Table 6–4. Approved 155–MB Winchester Disk Drive Specifications

Operating Characteristics (Unformatted)	Micropolis 1355
Transfer rate (MB/second)	10
Single cylinder seek time (typical)	5 msec
1/3 stroke seek time (typical)	31 msec
Maximum stroke seek time (typical)	62 msec
Average latency	8.33 msec
Sectors per track	18
Formatted sectors	147,312
Number of data heads	8
Nominal rpm	3600

Table 6–5. Approved 348–MB Winchester Disk Drive Specifications

Operating Characteristics (Unformatted)	Maxtor EXT–4380
Transfer rate (MB/second)	10
Single cylinder seek time (typical)	4 msec
1/3 stroke seek time (typical)	30 msec
Maximum stroke seek time (typical)	58 msec
Average latency	8.33 msec
Sectors per track	18
Formatted sectors	147,312
Number of data heads	8
Nominal rpm	3600

NOTICE: The specifications set forth in Tables 6–6 and 6–7 should be met under all combinations of operating environment and dc supply voltages.

6.4.1 Capacities

Table 6–6 lists the Winchester disk drive unformatted capacity specifications.

Table 6–6. Winchester Disk Unformatted Capacity Specifications

Specification	72 MB (DS3000 only)	155 MB	348 MB
Capacity	85 MB	170 MB	380 MB
Capacity per track	10,416 bytes	20,832 bytes	20,808 bytes
Number of cylinders	1024	1023	1023
Number of heads	8	8	8
Format (reference only)	9 sectors/track 1114 bytes/sector	18 sectors/track 1117 bytes/sector	18 sectors/track 1117 bytes/sector

6.4.2 Seek Time

Seek times on the 72–MB drive are measured from the first step pulse until "SEEK COMPLETE" becomes true. Seek operations use the buffered seek mode with a step pulse period of 6 microseconds, including head settling time. Seek times on the 155–MB and 348–MB drives are measured from the issuance of "SEEK" until "COMMAND COMPLETE" is issued.

6.4.3 Spindle/Disk Times

Table 6–7 lists the time specifications for Winchester disk drives.

Table 6–7. Winchester Disk Spindle/Disk Times

Specification	Time
Rotational speed	3600 rpm (± 0.5%)
Index period	16.67 msec (± 0.5%)
Start time (to "READY")	25 seconds maximum
Stop time	25 seconds maximum

Figure 6–4 shows the timing diagrams for the 72–MB Winchester disk drive operations.

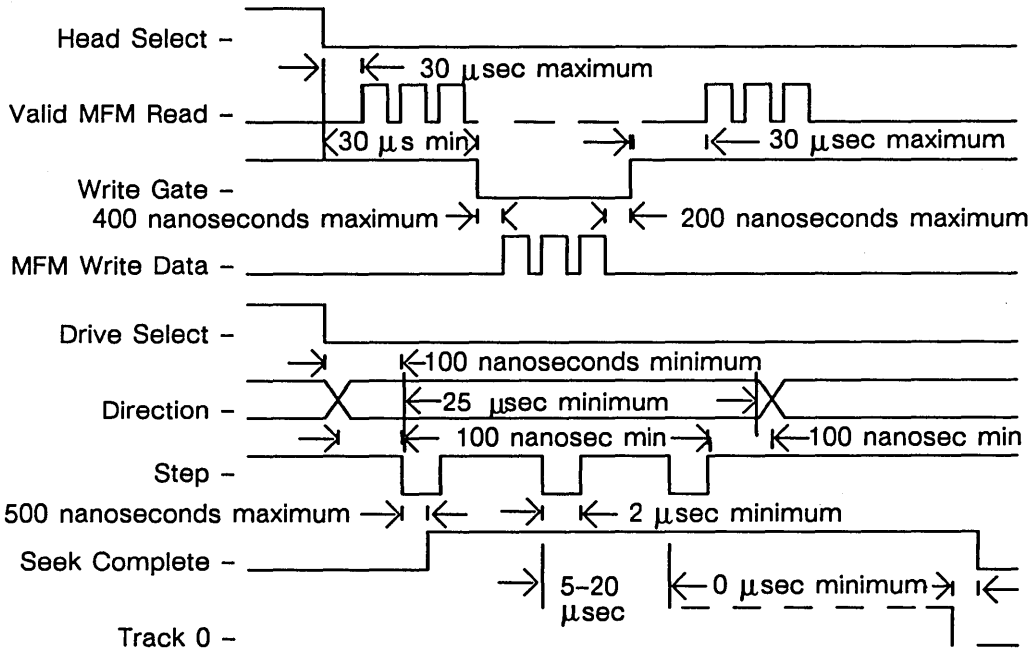


Figure 6–4. Winchester Interface Timing Diagrams

For 155–MB and 348–MB drive timing diagrams, consult the ESDI Interface Specification (Revision F).

6.4.4 Data Reliability

Table 6–8 lists the data reliability for the Winchester disk drives, excluding media defects.

Table 6–8. Winchester Disk Drive Data Reliability

Item	Specification
Window margin	20 nanoseconds minimum (Wilson MWX–1000 tester or equivalent) (72–MB drive only)
Soft read errors	Less than 1 per 10 to the tenth bits read (8 retries)
Hard read errors	Less than 1 per 10 to the twelfth bits read (8 retries)*
Seek errors	Less than 1 per 10 to the sixth seeks (no retries)
* May use any combination of track offset strobes (155–MB drive)	

6.4.5 Thermal Stabilization

The drive should meet the data reliability requirements as long as "READY" is true, with no required stabilization time and no regard to the particular environmental conditions under which the data was written, as long as it was within the Operating Range specified in Section 6.8.

6.4.6 Media Defects

The manufacturer should identify all media defects and provide a list of their locations by cylinder, head, and bytes from index. This list should be permanently attached to the drive. These defects, plus any

unlisted ones discovered during further testing, should be excluded from read error rate measurements. No single defect should be greater than 6 bytes long. However, multiple occurrences within 50 bytes of each other on a track will be counted as one defect when accounting for the limits in Table 6-9.

Table 6-9. Winchester Disk Drive Media Defect Limitations

Specification	72 MB (DS3000 only)	155 MB	348 MB
Defects per drive	85 maximum	170 maximum	380 maximum
Defects per surface	25 maximum	50 maximum	50 maximum
Number of heads	5 maximum	5 maximum	5 maximum
Defects on cylinder 0	None allowed	None allowed on heads 0, 1, 2, 3, 4	None allowed on heads 0, 1, 2, 3, 4

6.5 Power Specifications

See Figure 6-3 for the dc power connector pin assignments. The mating cable connector is the AMP 1-480424 with pins, the AMP 350078-4, or the equivalent. Tables 6-10 and 6-11 contain the power specifications for the DS3000 Winchester disk drives.

Table 6-10. 72-MB Winchester Disk Drive Power Specifications

Item	Specification
+5 Volts	± 5%, 100 mV maximum peak-to-peak ripple; 1.5 amp maximum
+12 Volts	± 5%, 240 mV maximum peak-to-peak ripple; 2.5 amps average (seeking)
Average Power Dissipation	40 watts maximum (seeking)
Cooling Required	Natural convection as required to maintain the ambient temperature range specified in Section 6.8.
Grounds	The external mounting frame is electrically insulated from the PCB ground. The HDA must be connected to the PCB ground to provide noise shielding. The HDA also has a spade lug connection (for mating AMP connector 62187-1 or its equivalent). No external connection to this lug is required for operation within these specifications.

Table 6-11. 155-MB and 348-MB Winchester Disk Drive Power Specifications

Item	Specification
+5 Volts	± 5%, 100 mV maximum peak-to-peak ripple; 1.5 amp maximum
+12 Volts	± 5%, 120 mV maximum peak-to-peak ripple; 2.5 amps average (seeking)
Average Power Dissipation	32 watts maximum (seeking)
Cooling Required	Natural convection as required to maintain the ambient temperature range specified in Section 6.8.
Grounds	The external mounting frame is electrically insulated from the PCB ground. The HDA must be connected to the PCB ground to provide noise shielding. The HDA also has a spade lug connection (for mating AMP connector 62187-1 or its equivalent). No external connection to this lug is required for operation within these specifications.

6.6 Mechanical Specifications

Figure 6–5 shows the dimensions and mounting hole locations for the Winchester disk drives.

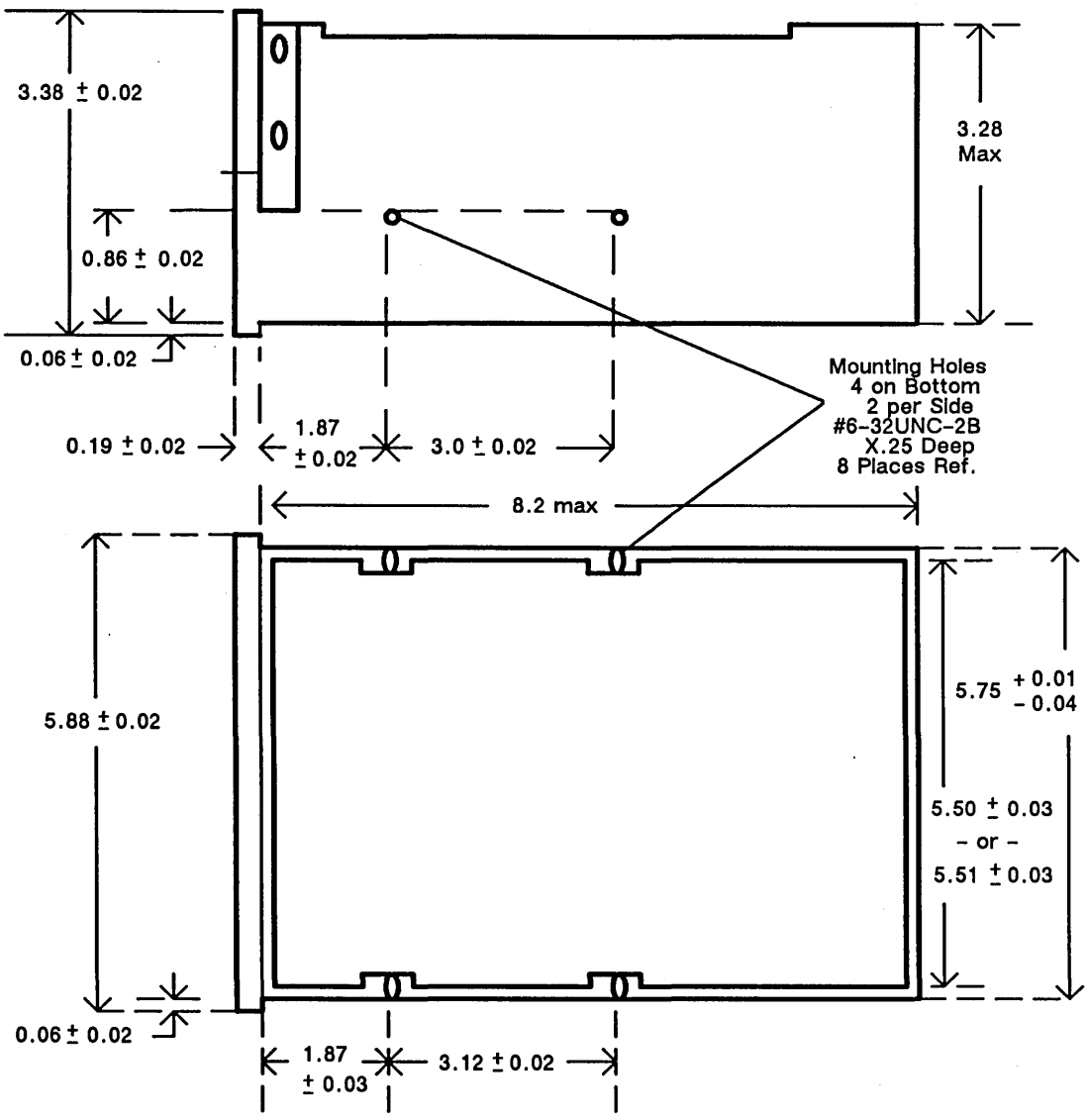


Figure 6–5. Winchester Disk Drive Dimensions

Drive Orientation: The drive can be positioned horizontally (mounting holes down) or vertically (on either long side), without reformatting the media.

Drive Weight: 72–MB drive – 8.5 pounds (maximum)
155–MB drive – 8.5 pounds (maximum)
348–MB drive – 7.5 pounds (maximum)

Acoustic Noise: The drive should produce less than 55 DBA (sound pressure) measured 3 feet from the drive while it is seeking.

Shock mounts for the disk drive should be attached within the package dimensions outlined in Figure 6–5.

6.7 Jumper Configurations

Figure 6–6 shows the jumper configurations on the various Winchester disk drives as they are used in the DS3000 and DS4000.

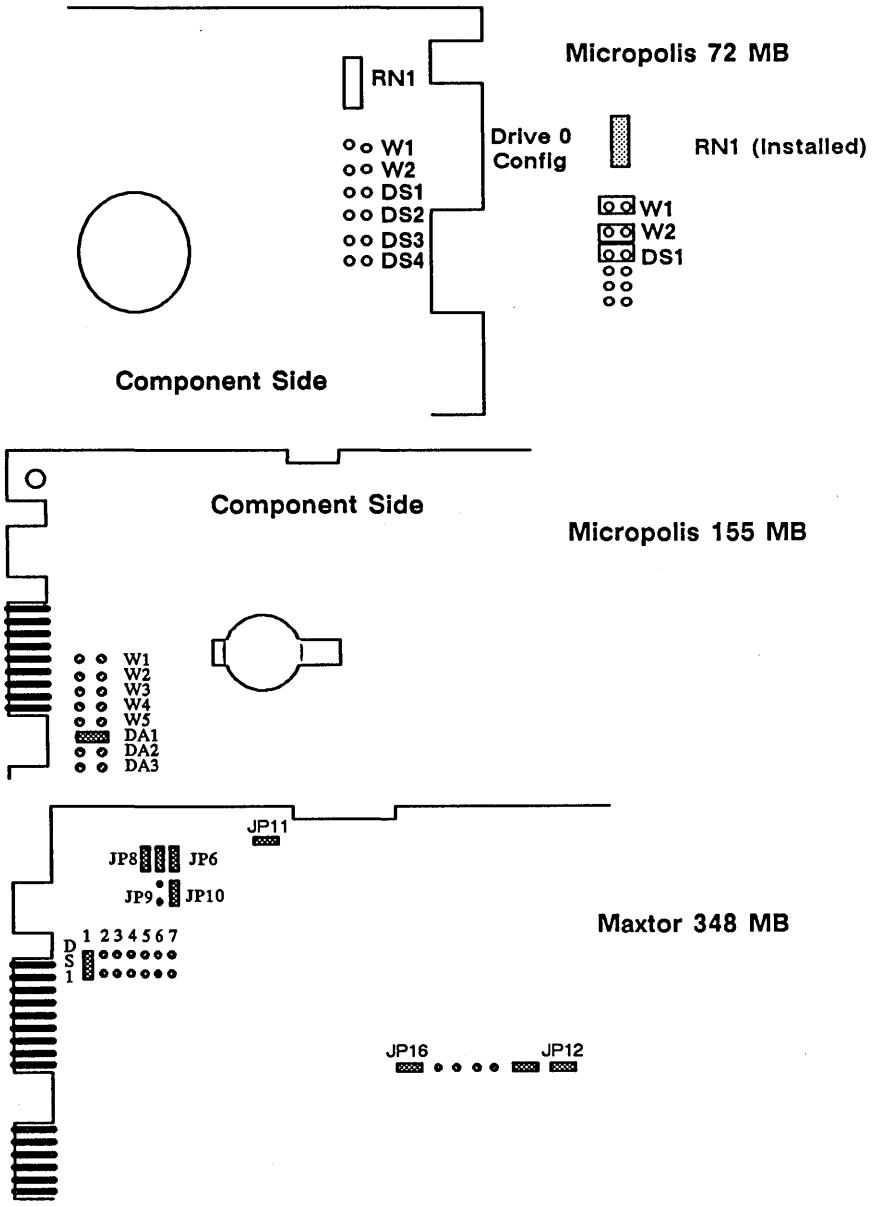


Figure 6–6. Winchester Disk Drive Jumper Configurations

6.8 Environmental Specifications

Subsections 6.8.1 through 6.8.3 list the environmental requirements for the Winchester disk drive.

6.8.1 Operating Environment

The Winchester drive should operate under any combination of the following conditions:

Ambient Temperature:	10 degrees C to 46 degrees C (50 degrees F to 115 degrees F)
Relative Humidity:	10% to 80% (noncondensing)
Wet Bulb:	26.7 degrees C (80 degrees F) maximum
Temperature Transient:	2 degrees C (3.6 degrees F) per 5 minutes maximum, 10 degrees C (18 degrees F) per 1 hour maximum (without condensation)
Altitude:	-200 to 10,000 feet above sea level
Vibration:	6 to 22 Hz, 0.01 inch peak-to-peak, 22 to 500 Hz, 0.25 G peak
Shock:	2 G peak, 11 msec 1/2 sinewave

The vibration and shock conditions are measured at the external mounting chassis. The temperature conditons are measured in still air at a 1 inch minimum from all surfaces.

6.8.2 Nonoperating (Unpackaged) Environment

The drive should withstand any combination of the following conditions in a powered-off state without damage or degradation to life expectancy:

Ambient Temperature:	-40 degrees C to 60 degrees C (40 degrees F to 140 degrees F)
Relative Humidity:	10% to 80% (noncondensing)
Wet Bulb:	26.7 degrees C (80 degrees F) maximum
Temperature Transient:	10 degrees C (18 degrees F) per 1 hour maximum (without condensation)
Altitude:	-1000 to 40,000 feet above sea level
Vibration:	6 to 22 Hz, 0.02 inch peak-to-peak, 22 to 500 Hz, 0.5 G peak
Shock:	20 G peak, 11 msec 1/2 sinewave, 0.75 inch free-fall drop

The vibration and shock conditions are measured at the external mounting chassis. The temperature conditons are measured in still air at a 1 inch minimum from all surfaces.

6.8.3 Shipping (Packaged) Environment

When packaged in the vendor's original shipping container, the drive should withstand (without functional or cosmetic damage) three 24-inch, free-fall drops onto every face, edge, and corner of the shipping container. Environmental conditions are specified with the following extensions:

Temperature Transient:	24 degrees C (43 degrees F) per 1 hour maximum
Vibration:	5 to 10 Hz, 0.2 inch peak-to-peak 10 to 44 Hz, 1 G peak 44 to 98 Hz, 0.01 inch peak-to-peak 98 to 300 Hz, 5 G peak
Shock:	50 G peak, 20 msec 1/2 sinewave, 24-inch, free-fall drop

Chapter 7

Floppy Disk Drive

7.1 Introduction

This chapter lists the requirements for the 5 1/4-inch, half height, high-density floppy disk drive, which provides 1.2 MB (formatted) of storage for the Series 3000 and Series 4000. Figure 7-1 shows the location of the floppy disk drive in the *Domain System* unit.

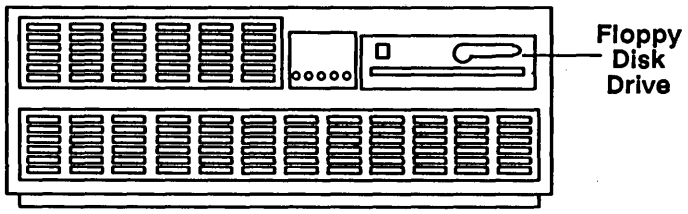


Figure 7-1. Domain System Unit

7.2 Required Design Features

This floppy disk drive must:

- Be capable of storing 1.2 MB of formatted data (in the high-density mode).
- Comply with the performance specifications set forth in this chapter.
- Be front-loading with a form factor and mounting holes that are compatible with industry-standard, half-height, 5-1/4-inch floppy disk drives.
- Operate in high-density mode at 360 rpm, with a data transfer rate of 500 Kb/sec.

- Use only +5 V dc and +12 V dc power, with no power sequencing required.
- Have dual recording heads to allow recording on both sides of the media.
- Reliably prevent any erasure or overwriting of data recorded on a write-protected disk.
- Have a jumper option to set its device number to 1, 2, 3, or 4.
- Have a Disk Changed output signal on pin 34 of the interface connector (see Section 7.6).

7.3 Performance Specifications

The Floppy Disk Drive (FDD) has an input signal on pin 2 of the interface connector for switching to and from high and normal density (if the drive has dual-density capabilities). In the high density mode, the FDD is equivalent to an 8-inch, double-sided, double-density flexible disk drive in data storage capacity and data transfer rate. During system operation, the floppy disk drive is always used in the high-density mode.

Table 7-1 lists the floppy disk drive's performance specifications in the high-density mode.

Table 7-1. Floppy Disk Drive Performance Specifications

Characteristic	Specification
Data Capacity (unformatted)	1.6 MB
Data Transfer Rate (bits/sec)	500K
Disk Rotation Speed	360 rpm (± 2%)
Tracks Per Inch (TPI)	96 TPI
Media	HD/2S
Sides	2
Cylinders	80
Tracks	160
Recording Method	MFM
Bit Density (bits/inch)	9646
Transfer Rate (bits/second)	500K
Access Times (maximum values):	
Track-to-Track	3 msec
Seek Settling Time	15 msec
Head Load Time	35 msec
Average Latency Time	83.3 msec
Start Time (maximum)	500 msec
Index to Data Burst Time	200 (+ 200/ - 160 μsec)

Since it is impossible for the floppy disk drive to identify which type of disk is installed, the floppy/disk controller identifies the type of media installed.

7.4 Physical Specifications

Figure 7–2 shows the exterior dimensions of the floppy disk drive.

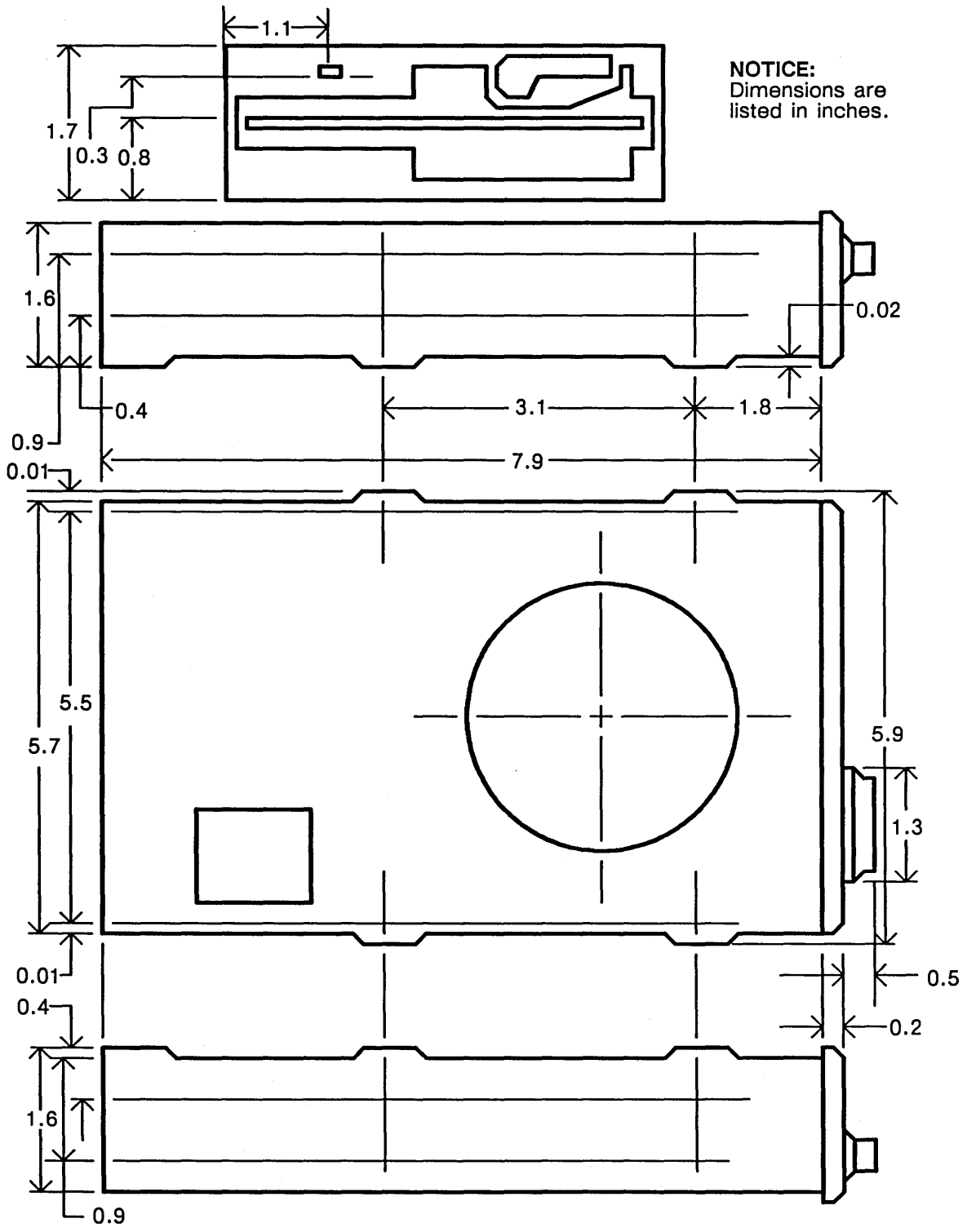


Figure 7–2. Floppy Disk Drive Exterior Dimensions

Any floppy disk drive used in the *Domain System* should conform to the following size specifications:

- Width: 146 mm (5.75 inches), nominal
- Height: 41.3 mm (1.63 inches), nominal
- Depth: 203 mm (7.99 inches), nominal (excludes the projections of interface connectors and the projection of the front bezel out of the package)
- Weight: 1.5 Kg (3.31 lb) or less
- Cooling: Free convection
- Mounting: Mounting in the following positions is required:

  Front loading, mounted vertically

  Front loading, mounted horizontally, with the spindle motor down

  Mounting angle should be less than 10 degrees with the front bezel up
- Installation: With installation holes on the side frame or on the bottom frame of the drive

7.5 Power Requirements

The floppy disk drive must conform to the input power specifications presented in Table 7–2.

Table 7–2. Floppy Disk Drive Power Specifications

Voltage (V dc)	Tolerance	Amperage	Ripple Voltage (Maximum)
+12	±5%	0.5	200 mV Peak-to-Peak
+5	±5%	0.8	100 mV Peak-to-Peak

7.5.1 Power Consumption

The following list contains the power consumption information for *Domain System* floppy disk drives:

- Typical Operating Power Consumption: 8.5 watts
- Typical Waiting Power Consumption: 4.0 watts
- Power–On Sequence Power Consumption: Not required. The FDD should be equipped with a power reset circuit. The disk and the data on the disk will not be damaged by power–on or power–off.

7.5.2 Power Interface

Figure 7–3 shows the power input connector from the power supply to the floppy disk drive.

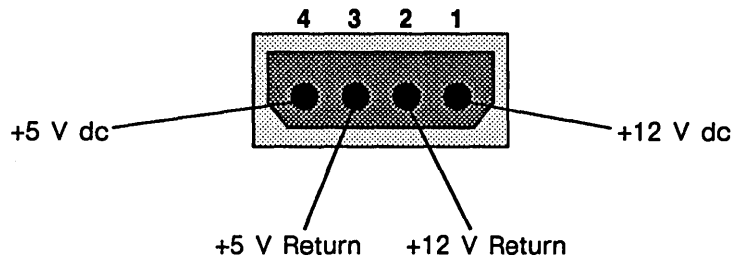


Figure 7–3. Floppy Disk Drive Power Supply Input Connector

The connector pictured in Figure 7–3 is an AMP connector (part number 1–480424–1). The mate for this input connector is an AMP connector (part number 1–480424–0).

7.6 Signal Interface and Definitions

The data and control line interface connector (3M part number 3463–001) links the floppy/disk controller to the 34–pin edge connector on the floppy disk drive PCB. On the connector, the odd–numbered contacts (1–33) are located on the noncomponent side of the floppy disk drive PCB. The even–numbered contacts (2–34) are located on the component side of the floppy disk drive PCB. Table 7–3 is a pin listing for the floppy disk drive PCB edge connector.

Table 7–3. Floppy Disk Drive PCB Edge Connector Pin Listing

Signal Name	Input/Output	Terminal Numbers	
		Signal	Return
HIGH/NORMAL DENSITY	Input	2	1
IN USE/HEAD LOAD	Input	4	3
DRIVE SELECT 3	Input	6	5
INDEX	Output	8	7
DRIVE SELECT 0	Input	10	9
DRIVE SELECT 1	Input	12	11
DRIVE SELECT 2	Input	14	13
MOTOR ON	Input	16	15
DIRECTION SELECT	Input	18	17
STEP	Input	20	19
WRITE DATA	Input	22	21
WRITE GATE	Input	24	23
TRACK 00	Output	26	25
WRITE PROTECT	Output	28	27
READ DATA	Output	30	29
SIDE ONE SELECT	Input	32	31
DISK CHANGED	Output	34	33

The following specifications are applicable for signals at the floppy disk drive edge connector:

Input Signal	LOW level (TRUE) – 0 V to 0.5 V Terminator current – 18 mA (maximum) Receiver TTL current – 3.2 mA (maximum) HIGH level (FALSE) – 2.5 V to 5.25 V (dependent on the controller terminator)
Output Signal	LOW level (TRUE) – 0 V to 0.5 V Driver sink current capability – 48 mA (maximum) HIGH level (FALSE) – 5.25 V (maximum) Terminator for DRIVE SELECT 0 (dependent on the controller terminator)

7.6.1 Signal Definitions

This subsection contains the signal definitions for floppy disk drive–to–disk controller communications.

High/Normal Density (DEN)

This signal is used to switch the recording density of the floppy disk drive.

In Use/Head Load (HLD)

The logic level for this signal is selected by setting jumpers on the drive. When Head Load is selected, setting HLD low causes the magnetic head to touch the disk's surface.

Drive Select 0 to 3 (DX0 to DX3)

Setting one of these signals enables the corresponding drive's I/O lines.

Motor On (MON)

Setting this signal low turns on the spindle motor when a diskette is loaded into the drive.

Direction Select (DIR)

This signal indicates the direction of the magnetic head movement. When DIR is high, the head moves toward the outer tracks. When DIR is low, the head moves toward the inner tracks.

Step (STP)

The pulsed Step signal moves the magnetic head in the direction specified in the Direction Select signal. The head moves over one cylinder for each Step pulse.

Write Data (WDT)

This signal supplies the drive with the data to be written on the diskette. Each time the signal changes from high to low, the current flowing in the magnetic head changes direction. This changes the magnetization on the disk.

Write Gate (WGT)

When this signal is low, data can be written to the diskette. When WGT is high, data can only be read from the diskette.

Side One Select (SSL)
This signal selects one of the heads to be used in a Read/Write operation. When SSL is high, the magnetic head on Side 0 of the diskette is selected. When SSL is low, the magnetic head on Side 1 of the diskette is selected.

Index (IDX)
This signal indicates the starting point of Track 0 on the diskette, one time per rotation.

Track 00 (TK0)
This signal, when low, indicates that the heads are on Track 00.

Write Protect (PRT)
This signal goes low if the write protect notch on the diskette is covered (write protected).

Read Data (RDT)
When this signal is low, data can be read from the diskette.

Disk Changed (DCG)
The drive sends this signal to the controller, warning that the diskette has been removed from the drive.

7.6.2 Input Signal Termination

The following specifications apply to the input signals listed in Table 7–3:

- Resistance value: 150 to 330 ohms (± 5%).
- Terminator for DRIVE SELECT 0 through 3 input signal: A terminator resistor must be used.
- Terminator for Other Input Signals: A resistor network can be mounted in an IC socket on the PCB.

7.6.3 Multiplexed Connections

For daisy–chaining up to four floppy disk drives, the resistor network referenced in Subsection 7.6.2 will be removed from the first three drives. It will, however, remain in the last drive on the chain.

7.6.4 Signal Connector

The pins on the floppy disk drive PCB edge connector should conform to the following specifications:

- Floppy disk drive signal connector – card edge (gold plated)
- Pin numbers and pin pitch – 34 pins, 2.54–mm (0.1–inch) pitch (17 pins on both sides)
- Polarizing key location – between pins 4 and 6
- Interface connections – see Table 7–3
- Ribbon cable side mating connector – 3M Scotchflex ribbon connector (P/N 3463–0001) or AMP thin leaf connector (P/N 583717–5) and contactor (P/N 1–583616–1) or equivalent

Figure 7–4 shows the ribbon cable connections to the floppy disk drive and disk controller.

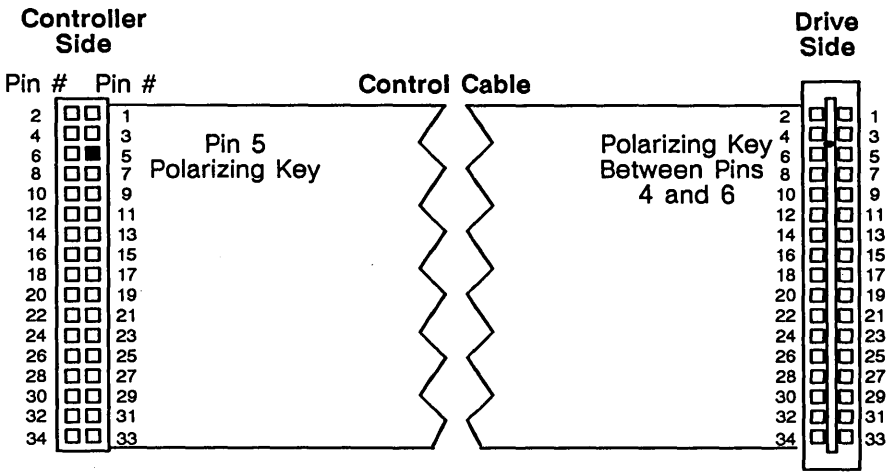


Figure 7–4. Floppy Disk Drive Ribbon Cable Connectors

7.6.5 Maximum Interface Cable Length

The cable from the floppy disk drive PCB edge connector to the disk/floppy controller PCB should conform to the following specifications:

- Length: 3 meters (9 feet, 10 inches) maximum.
- For the multiplex connection by daisy-chaining, the total cable length must be less than 3 meters (9 feet, 10 inches).

7.7 Floppy Disk Drive Component Specifications

Subsections 7.7.1 through 7.7.8 describe the specifications for the major floppy disk drive components.

7.7.1 Disk Rotation Mechanism

Table 7–4 lists the specifications for the floppy disk drive rotation mechanism.

Table 7–4. Floppy Disk Drive Rotation Mechanism Specifications

Characteristic	Specification
Spindle Motor	Direct dc brushless motor
Motor Servo Method	Frequency servo by ac tachometer
Motor/Spindle Connection	Motor shaft direct
Long Term Speed Variation	Less than ± 1.5%
Instantaneous Speed Variation	Less than ± 1.5%
Speed Change Time	Less than 400 msec (from 300 to 360 rpm)
Characteristic	**High Density**
Start Time	Less than 500 msec
Disk Speed	360 rpm
Average Latency	83.3 msec
Spindle Motor Speed	360 rpm

7.7.2 Index Mechanism

Table 7–5 lists the specifications for the floppy disk drive index mechanism.

Table 7–5. Floppy Disk Drive Index Mechanism Specifications

Characteristic	Specification
Number of Index	One per disk revolution
Detection Method	LED or phototransistor
Characteristic	**High Density**
Detection Cycle	166.7 msec (± 1.5%)
Index Burst Detection Timing Tolerance (with specified disk test)	±165 μsec maximum

7.7.3 Magnetic Head

Table 7–6 lists the specifications for the floppy disk drive magnetic head.

Table 7–6. Floppy Disk Drive Magnetic Head Specifications

Characteristic	Specification
Magnetic Head	Gimball supported read/write head with tunnel erase
Read/Write Track Head Width	0.165 inch nominal
Track Width After Tunnel Erase	0.155 (±0.015) mm; 0.0061 (± 0.0006) inch
Erase Head Track Width	0.095 mm (0.0037 inch) both sides nominal
Read/Write–Erase Gap Spacing	0.585 (±0.05) mm; 0.0230 (± 0.0020) inch
Read/Write Gap Azimuth	0 degrees (± 18) with specified disk test

7.7.4 Track Seek Mechanism

Table 7–7 lists the specifications for the floppy disk drive Track Seek mechanism.

Table 7–7. Floppy Disk Drive Track Seek Mechanism Specifications

Characteristic	Specification
Head Carriage Drive Mechanism	Stepping motor and steel belt
Stepping Motor	4–phase, 200 steps per revolution
Stepping Motor Drive	One step per track for 96 TPI
Track 00 and Innermost Stopper	Mechanical crash stops to prevent head damage or alignment shift.
Track–to–Track Time	3 msec minimum
Settling Time	Less than 15 msec (excluding track–to–track time)
Average Track Access Time (including settling time)	94 msec (for 80 cylinders)

7.7.5 Head Load Mechanism

The *Domain System* does not require a head load solenoid. If the drive has one, it must have a head load time of less than 50 milliseconds. Also, if it has a head load solenoid, the head load function must be selectable as a result of:

- The Head Load signal from the controller and Drive Select asserted, or
- The Motor On signal from the controller and Drive Select asserted.

7.7.6 File Protect Mechanism

The floppy disk drive uses an LED or phototransistor to detect the write protect notch on the floppy disk.

7.7.7 Window Margin

Using specified test media with a Brikon (or equivalent) tester and no write precompensation, this is the specified window margin:

High Density: 500 nanoseconds minimum at track 79

7.7.8 Write Precompensation

The floppy disk drive should be capable of operating in high-density mode with no problems, and use up to 200 nanoseconds of write precompensation.

7.8 Environmental Conditions

Table 7-8 lists the environmental specifications for the floppy disk drive while it is operating.

Table 7-8. Floppy Disk Drive Environmental Specifications (Operating)

Characteristic	Specification
Temperature	50° to 113° F or 10° to 45° C
Temperature Gradient	18° F or 10° C
Relative Humidity	20 to 80% RH noncondensing with a maximum wet bulb temperature of 77° F or 29° C
Relative Humidity Gradient	20% change per hour maximum
Vibration (sweep rate of 1 octave/minute)	0.01 inch DA, 5 to 22 Hz 0.25 G, 22 to 500 Hz
Shock	Less than 10 G (11-msec pulse duration)
Altitude	Less than 16,500 feet (5,000 meters)

Table 7–9 lists the environmental specifications for the floppy disk drive while it is packaged.

Table 7–9. Floppy Disk Drive Environmental Specifications (Packaged)

Characteristic	Specification
Temperature	–8° to 140° F or –22° to 60° C
Temperature Gradient	54° F or 30° C per hour
Relative Humidity	8 to 90% RH noncondensing with a maximum wet bulb temperature of 104° F or 40° C
Relative Humidity Gradient	20% change per hour maximum
Vibration (sweep rate of 1 octave/minute)	Less than 3 G, 5 to 100 Hz
	Less than 0.5 G, 100 to 500 Hz
	Less than 0.5 G, 500 to 100 Hz
	Less than 3 G, 100 to 5 Hz
Shock	Less than 40 G (11–msec pulse duration)
Altitude	Less than 40,000 feet (12,000 meters)

Table 7–10 lists the environmental specifications for the floppy disk drive while it is being transported.

Table 7–10. Floppy Disk Drive Environmental Specifications (Transporting)

Characteristic	Specification
Temperature	–40° to 158° F or –40° to 70° C
Relative Humidity	5% to 95% RH noncondensing with a maximum wet bulb temperature of 113° F or 45° C
Altitude	Less than 40,000 feet (12,000 meters)

Chapter 8

Cartridge Tape Controller

8.1 Introduction

This chapter describes the electrical, physical, and environmental specifications for the *Domain System* cartridge tape controller. The controller provides the interface between a QIC-36, 1/4-inch, cartridge tape drive (basic interface) and an IBM PC/AT, QIC-02 I/O structured compatible system. Figure 8-1 shows the tape controller.

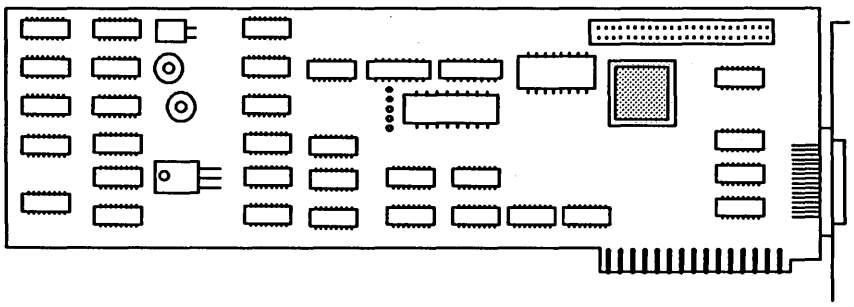


Figure 8-1. Cartridge Tape Controller

8.2 Relevant Documentation

For additional information, refer to the following documents:

- *1/4-inch Cartridge Tape Drive Basic Interface*, QIC-36 Revision C, 9/14/84
- *Proposed Standard for Data Interchange on the Streaming 1/4-Inch Magnetic Tape Cartridge Using Group Code Recording at 10,000 FRPI*, QIC-24 Revision D, 4/22/83
- Specification - *Tape Controller Information Guide*, Archive Corp., SC-499 (preliminary)
- *Specification - 1/4" Cartridge Tape Drive Interface Standard*, QIC-02, Rev. D, 8/23/82
- *Theory of Operation - Intelligent 1/4" Tape Drive*, Archive Corp., Rev. C #20100-001, 8/16/82

8.3 Physical Specifications

Subsections 8.3.1 through 8.3.3 contain the physical specifications for the cartridge tape controller.

8.3.1 Physical Parameters

The cartridge tape controller has the following physical specifications:

- Width: 34.29 cm (13.5 in)
- Height: 10.67 cm (4.2 in)
- Weight: 0.27 Kg (0.6 lb)

Refer to Figure 8–2 for a complete illustration of the physical layout of the tape controller, including jumpers, connectors, and diagnostic LED indicators.

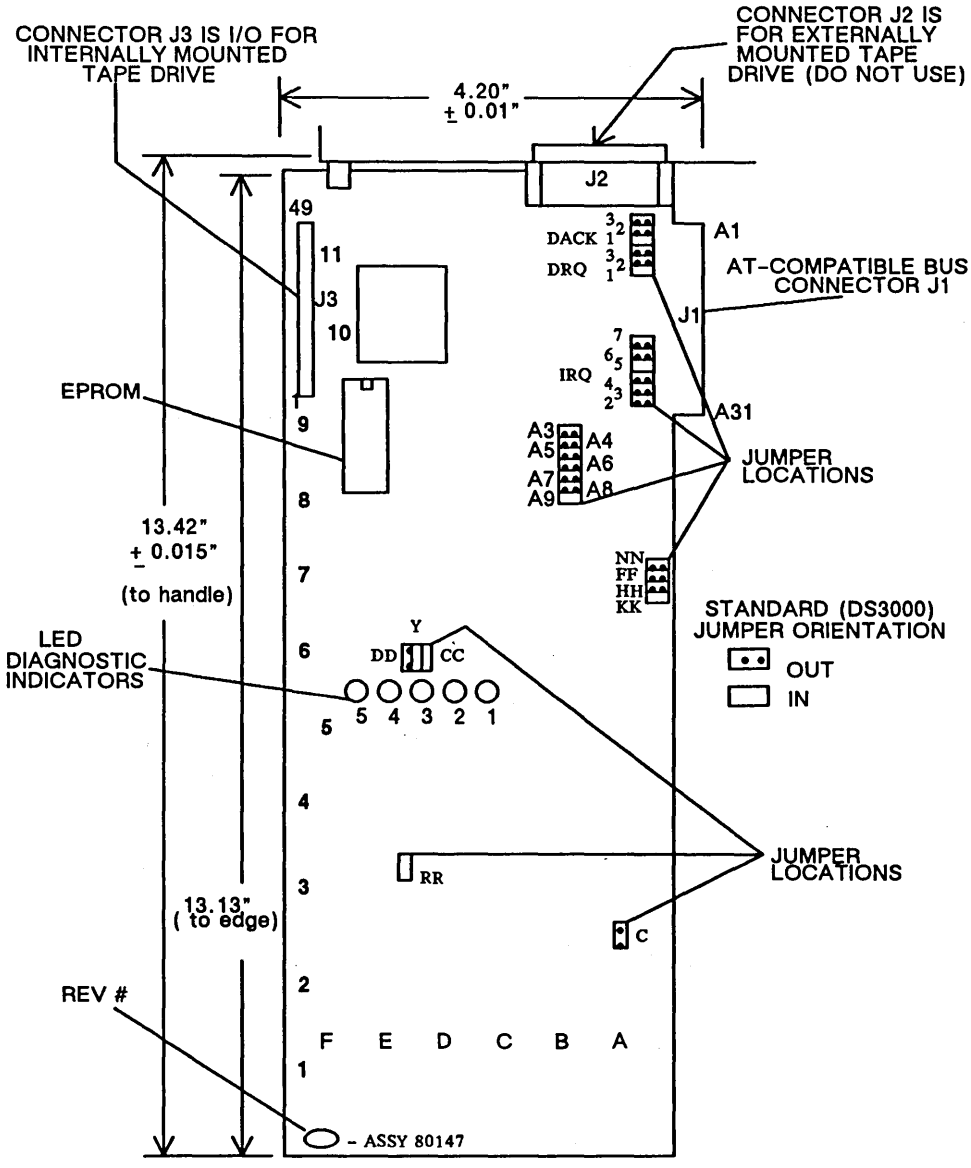


Figure 8–2. Cartridge Tape Controller Physical Layout

8.3.2 Jumper Configurations

Table 8-1 describes the functions of the jumpers on the tape controller board. The tape controller must be configured as follows to avoid bus contention between the tape controller and any other controller using the AT-compatible bus:

Device Address (base address)	218 (hex)
DMA Channel	1
Interrupt Request Level	5

Table 8-1. Tape Controller Jumper Configurations

Description	Jumper Location	Option
Tape Format	CC	IN = QIC-24 * ● OUT = QIC-11
Tape Speed	DD	OUT (90 ips) * ● (for vendor use only)
Number of Tracks	Y	IN = 9 Tracks* ● OUT = 4 Tracks
Power-On Confidence Test	KK	IN = Test at Power-On* ● or Reset OUT = Test Disabled
I/O Register Base Address	A3 THRU A9 A3 THRU A8 = OUT* ● A9= IN* ●	IN = Address Bit True OUT = Address Bit False NOTICE: Base Address is selectable from 0 to 3F8 (hex) on 8-byte boundaries.
DMA Priority Level (Select One Pair)	DRQ1, DACK1 DRQ2, DACK2 DRQ3, DACK3	BOTH IN = Priority Level 1 * ● BOTH IN = Priority Level 2 BOTH IN = Priority Level 3
Interrupt Priority	IRQ2 IRQ3 IRQ4 IRQ5 IRQ6 IRQ7	IN = Priority Level 2 IN = Priority Level 3 ● IN = Priority Level 4 IN = Priority Level 5* IN = Priority Level 6 IN = Priority Level 7
Loop On Error	FF	OUT* ● = (for vendor use only)
Maintenance	C	OUT* ● = (for vendor use only)
Test Configuration	HH	OUT* ● = (for vendor use only)
No Description	NN	OUT* ● = (for vendor use only)
Ready Interrupt	RR RR	OUT ● = READY (and DONE) enabled IN* = READY disabled when DONE INT. enabled or READY enabled when DONE INT. disabled

● Configuration from vendor. * DS3000 configuration only.

8.3.3 Diagnostic LEDs

The tape controller performs a set of basic diagnostic tests at power-on and when the *Domain System* issues a RESET. The controller uses its set of five LEDs (see Table 8-2) to indicate a pass or fail from the diagnostics. All five LEDs light when the tests begin, and then shut off when the controller successfully passes the tests. A flashing LED indicates a failure. Table 8-2 shows the LED failure codes.

Table 8-2. LED Diagnostic Failure Codes

Flashing LED	Failure
5 4 3 2 1 ○ ○ ○ ○ ●	LSI Controller chip
○ ○ ○ ● ○	16K RAM Buffer Logic
○ ○ ● ○ ○	Data Seperator Logic

8.4 Power Requirements

Table 8-3 shows the voltages and currents required to operate the tape controller.

Table 8-3. Tape Controller Power Specifications

Voltage (V dc)	Tolerance	Amperage	Ripple Voltage (Maximum)
+5	±5%	1.5	100 mV
+12	±5%	0.1	500 mV to 10 KHz 200 mV beyond 10 KHz

8.5 Tape Drive Interface and Descriptions

The tape controller must support a QIC-36 (basic interface) compatible tape drive and must meet the specifications for the QIC-36 interface as referenced in the documents listed in Section 8.2.

The physical interconnections between the drive and controller are made via card-connector J3 on the controller (see Figure 8-2) over a 3M-type 3365/50 flat ribbon cable terminated with a CA-50 IDS socket. The maximum interface cable length is 3 meters (10 feet).

8.5.1 Controller-to-Drive Interface Signals

All interface signals between the basic tape drive and the controller are TTL logic levels defined as follows:

Signals From Drive:

Signal True = Logic 1 (Low) 0.0 to 0.55 V dc
Signal False = Logic 0 (High) 2.40 to 5.25 V dc

Signals To Drive:

Signal True = Logic 1 (Low) 0.0 to 0.80 V dc
Signal False = Logic 0 (High) 2.00 to 5.25 V dc

All signals from the tape drive to the controller are capable of driving one standard TTL load (1.6 mA) in addition to the 23 mA required by the tape drive interface terminations. Refer to the documents listed in Section 8.2 for more information.

All signals passed between the controller and drive must be terminated with 330 ohms (± 5%) to ground, and 220 ohms (± 5%) to 5 V dc. Signal inputs to the controller must be terminated at the controller. Signal outputs from the controller are terminated at the drive. Figure 8–3 shows the signal termination scheme.

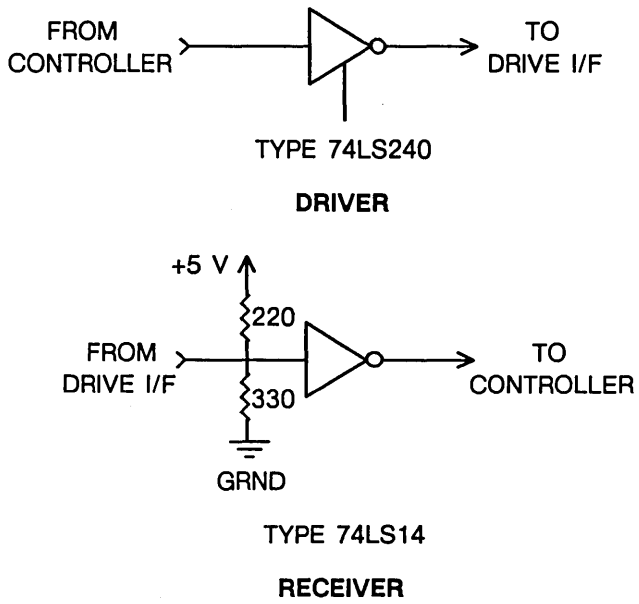


Figure 8–3. Signal Termination Scheme

Table 8-4 shows the pin assignments for connector J3 on the controller board. (These pin assignments correspond one-for-one with the pin assignments on the tape drive.)

Table 8-4. Tape Controller J3 Connector Pin Listing

J3 Pin No.	Signal Name	I/O	Signal Description
02	GO-	D	Go Control for Capstan Servo
04	REV-	D	Direction Control for Capstan Servo
06	TR3-	D	Track Select Bit 3
08	TR2-	D	Track Select Bit 2
10	TR1-	D	Track Select Bit 1
12	TR0-	D	Track Select Bit 0
14	RST-	D	Reset
16	RES	D	Reserved for future use
18	RES	D	Reserved for future use
20	RES	D	Reserved for future use
22	DS0-	D	Drive 0 Select Control
• 24	HC-	D	High write current for DC-600 tape
26	RDP-	C	Read Pulse Output - one pulse per flux transition
28	UTH-	C	Upper Tape Position Code
30	LTH-	C	Lower Tape Position Code
• 32	SLD-	C	Response from Drive when selected
34	CIN-	C	Cartridge In Place
36	USF-	C	Unsafe - File Protect Plug is in Unsafe Position (Writing is enabled)
38	TCH-	C	Capstan Tachometer Pulses
40	WDA-	D	Write Data Signal
42	WDA+	D	Inverse Write Data Signal
• 44	THD-	D	Threshold- % qualifying amplitude for read signal off tape
• 46	HSD-	D	High Speed- selects tape speed of 90 ips
48	WEN-	D	Write Enable Control
50	EEN-	D	Erase Enable Control

C = Controller
D = Drive

• These signals are optional and are not required for compliance with this specification.

NOTICE: All odd-numbered pins are signal returns and connect to signal GND at the drive.

8.5.2 Controller-to-AT-Compatible Bus Signals

Refer to the description of the AT-compatible bus in Chapter 2 of this manual.

8.6 Environmental Conditions

Tables 8–5 and 8–6 list the environmental specifications for the tape controller. The controller must be capable of operating under any combination of the conditions in Table 8–5 without failure to meet all of the other specifications described in this chapter.

Table 8–5. Tape Controller Environmental Specifications (Operating)

Characteristic	Specification
Temperature	5 to 60 °C (41 to 140 °F)
Temperature Gradient	1 °C (1.8 °F) maximum per minute 20 °C (36 °F) maximum per hour noncondensing
Wet Bulb Temperature	26 °C (79 °F) maximum
Relative Humidity	0 to 99% noncondensing
Altitude	–1000 to 15,000 feet above sea level
Vibration	0 to 63 Hz, 0.005 inch peak-to-peak, 63 to 500 Hz, 1.0 G peak maximum
Shock	2.5 G peak (1/2 sine wave, 11–msec duration) on any axis)

The controller must be capable of withstanding any combination of the conditions in Table 8–6 without damage or degradation to life expectancy.

Table 8–6. Tape Controller Environmental Specifications (Nonoperating, Unpackaged)

Characteristic	Specification
Temperature	–30 to 60 °C (–22 to 140 °F)
Temperature Gradient	30 °C (54 °F) maximum per hour noncondensing
Wet Bulb Temperature	26 °C (79 °F) maximum
Relative Humidity	0 to 99% noncondensing
Altitude	–1000 to 15,000 feet above sea level 1 hour min. exposure unpackaged
Vibration	0 to 17 Hz, 0.1 inch peak-to-peak maximum, 17 to 500 Hz, 1.5 G peak maximum
Shock	2.5 G peak (1/2 sine wave, 11–msec duration) on any axis)

Chapter 9

Cartridge Tape Drive

9.1 Introduction

This chapter lists the requirements for a 1/4-inch cartridge tape drive with a basic interface and a half-height, 5 1/4-inch form factor (used with a QIC-36 compatible tape controller). The cartridge tape drive provides 45 or 60 MB of storage (with a 450- or 600-foot tape cartridge, respectively) for the *Domain System*. Figure 9-1 shows the location of the cartridge tape drive in the *Domain System* unit.

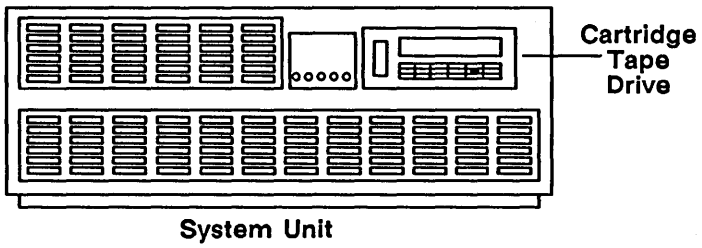


Figure 9-1. Domain System Unit with Cartridge Tape Drive

9.2 Relevant Documentation

For additional information, refer to the following documents:

1/4-inch Cartridge Tape Drive Basic Interface, QIC-36 Revision C, 9/14/84

Proposed Standard for Data Interchange on the Streaming 1/4-Inch Magnetic Tape Cartridge Using Group Code Recording at 10,000 FRPI, QIC-24 Revision D, 4/22/83

9.3 Required Design Features

The cartridge tape drive must provide the following functions (jumper options permissible):

- Unless otherwise noted, meet all of the requirements of the previously referenced QIC–36 Basic Interface Specification.
- Internally and automatically adapt its read and write circuits for proper operation with either normal or high–coercivity type tape.
- Internally and automatically invoke a 25% qualifying amplitude (threshold) for the Read signal during a Read–During–Write operation.
- Reliably prevent any erasure or overwriting of data recorded on a write–protected ("safe") cartridge, regardless of any sequence of power on/off and interface signals.
- Illuminate its front–panel indicator whenever the "Drive Select 0" interface signal is true.
- Provide an on–board interface signal termination network as specified in QIC–36.

9.4 Performance Specifications

The cartridge tape drive must meet the specifications described in this section and listed in Table 9–1 under all combinations of the operating environment and power supply voltages as specified elswhere in this chapter.

Table 9–1. Cartridge Tape Drive Performance Specifications

Characteristic	Value
Data Capacity (minimum)	45 MB (450–ft tape) 60 MB (600–ft tape)
Number of Tracks	9
Recording Density (nominal)	10,000 flux changes/inch 8000 bits/inch (GCR)
Transfer Rate (nominal)	90 KB/second
Tape Speed (long term)	90 inches/second ± 3%
Short–Term Speed Variation	± 7% as required to ensure compliance with QIC–24, Rev D, Data Interchange Standard
Start/Stop Time (maximum)	300 milliseconds
Rewind Time (maximum)	85 seconds (600–ft tape) 65 seconds (450–ft tape)
Track Selection Time (maximum)	600 milliseconds
Power–Up Initialization Time (maximum)	10 seconds at BOT 90 seconds at EOT
Recoverable Write Errors	Less than 500/cartridge
Unrecoverable Write Errors	None (16 retries)
Recoverable Read Errors	Less than 1/10**8 bits transferred (16 retries)
Unrecoverable Read Errors	Less than 1/10**10 bits transferred (16 retries)

The cartridge tape drive must also meet the following specifications:

Recording Head: Two-channel serpentine with read-after-write gaps and full-width erase bar.

Data Interchange: The tape drive must meet the read error rates listed in Table 9-1 without regard to its own environmental conditions or those of any other drive in which the cartridge was written, so long as both are within the operating range listed in the environmental specifications and both meet the thermal stabilization requirements that appear next, and so long as both interchanging drives and controllers comply with the QIC-24, Revision D, Data Interchange Standard.

Thermal Stablization: The tape drive must meet the read and write error rates listed in Table 9-1 and the data interchange requirement in the previous item with no stabilization time required after a power-on or after a cartridge is inserted; except that a Cartridge Initialization (retensioning) operation must be performed after a cartridge is inserted, and both the drive and cartridge must have been conditioned to the operating environment specified in this chapter for at least 4 hours, or the length of time they were outside that environment, whichever is shorter.

Electrostatic Discharge: The tape drive must continue to meet all the specifications described in this chapter, including the read and write error rates listed in Table 9-1, when subjected to an electrostatic discharge of 10,000 volts to any feature accessible from the front of the unit when installed in a DS3000 or DS4000 system unit. It must not suffer any permanent damage when subjected to an electrostatic discharge of 20,000 volts to the same features.

9.5 Physical Specifications

Any cartridge tape drive used in a *Domain System* should conform to the following specifications:

- Orientation: Horizontal with "Side A" down, or vertical on long side ("Side A" to left) without realigning the tape head (see Figure 9-2)
- Weight: 1.4 Kg (3 lb) maximum
- Cooling: Free convection
- Acoustic Noise: Less than 55 dBA (sound pressure) measured 3 feet from drive while streaming
- Cartridge Registration: Must comply with ANSI specification X3.55-1982
- Cartridge Lock: None required

Figure 9–2 shows the exterior dimensions and mounting holes of the cartridge tape drive.

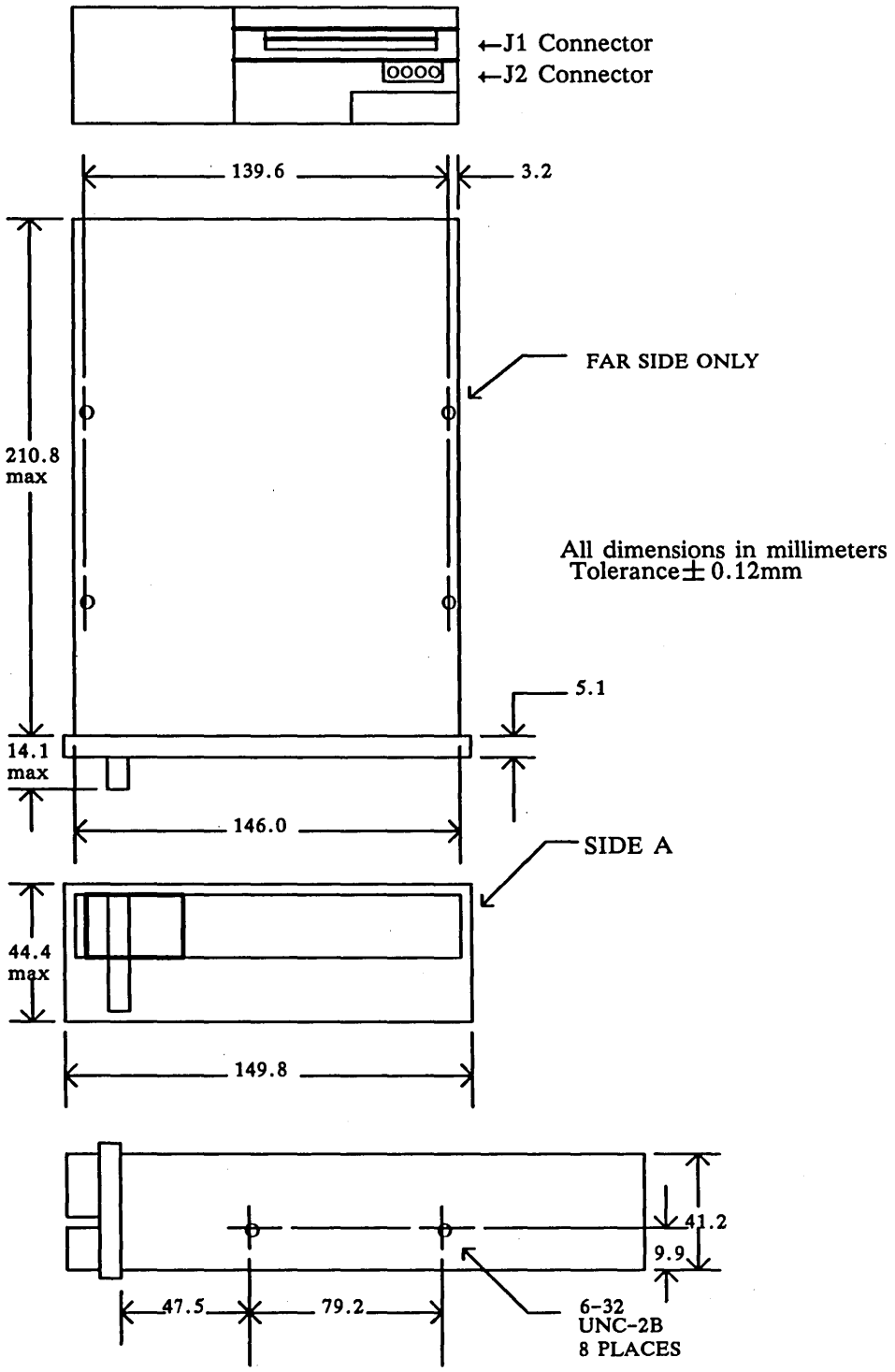


Figure 9–2. Tape Drive Exterior Dimensions and Mounting Holes

9.6 Power Requirements

The tape drive must conform to the input power specifications presented in Table 9–2.

Table 9–2. Tape Drive Power Specifications

Voltage (V dc)	Tolerance	Amperage	Ripple Voltage (Maximum)
+12	±5%	2.4	200 mV peak-to-peak
+5	±5%	0.6	100 mV peak-to-peak
Maximum peak-to-peak ripple current drawn by +12 V (> 1 kHz component) must be less than 1 amp.			

The tape drive does not requires voltage sequencing.

The drive chassis must be insulated from the electrical grounds in connector J2 (see Figure 9–3).

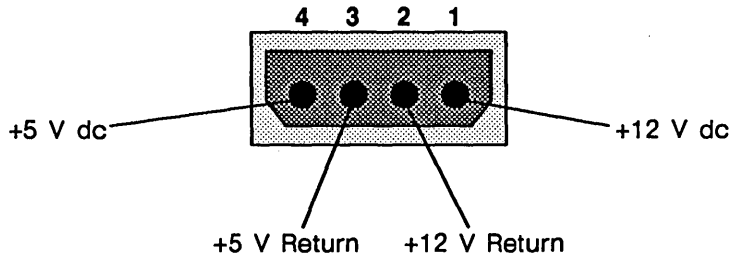


Figure 9–3. Tape Drive Power Supply Input Connector

The connector pictured in Figure 9–3 is an AMP connector (part number 1–480424–1). The mate for this input connector is an AMP connector (part number 1–480424–0).

9.7 Signal Interface and Descriptions

The data and control line interface connector (3M–type 3425) links the tape controller to the 50–pin edge connector on the tape drive PCB. On the connector, the odd–numbered contacts (1–49) are located on the noncomponent side of the tape drive PCB. The even–numbered contacts (2–50) are located on the component side of the tape drive PCB. Table 9–3 is a pin listing for the tape drive PCB edge connector. Signal definitions are according to QIC–36 with the exception of the "reserved" signals. The drive ignores any signals the controller places on the "reserved" signal lines. Figure 9–4 shows the cable connections.

Table 9-3. Tape Drive PCB Edge Connector Pin Listing

J1 Pin No.	Signal Name	I/O	Signal Description
02	GO–	D	Go Control for Capstan Servo
04	REV–	D	Direction Control for Capstan Servo
06	TR3–	D	Track Select Bit 3
08	TR2–	D	Track Select Bit 2
10	TR1–	D	Track Select Bit 1
12	TR0–	D	Track Select Bit 0
14	RST–	D	Reset
16	RES	D	Reserved for future use
18	RES	D	Reserved for future use
20	RES	D	Reserved for future use
22	DS0–	D	Drive 0 Select Control
• 24	HC–	D	High write current for DC-600 tape
26	RDP–	C	Read Pulse Output – one pulse per flux transition
28	UTH–	C	Upper Tape Position Code
30	LTH–	C	Lower Tape Position Code
32	SLD–	C	Response from Drive when selected
34	CIN–	C	Cartridge In Place
36	USF–	C	Unsafe – File Protect Plug is in Unsafe Position (Writing is enabled)
38	TCH–	C	Capstan Tachometer Pulses
40	WDA–	D	Write Data Signal
42	WDA+	D	Inverse Write Data Signal
• 44	THD–	D	Threshold– % qualifying amplitude for read signal off tape
• 46	HSD–	D	High Speed– selects tape speed of 90 ips
48	WEN–	D	Write Enable Control
50	EEN–	D	Erase Enable Control

C = Controller
D = Drive

• These signals are optional and are not required for compliance with this specification.

NOTICE: All odd-numbered pins are signal returns and connect to signal GND at the drive.

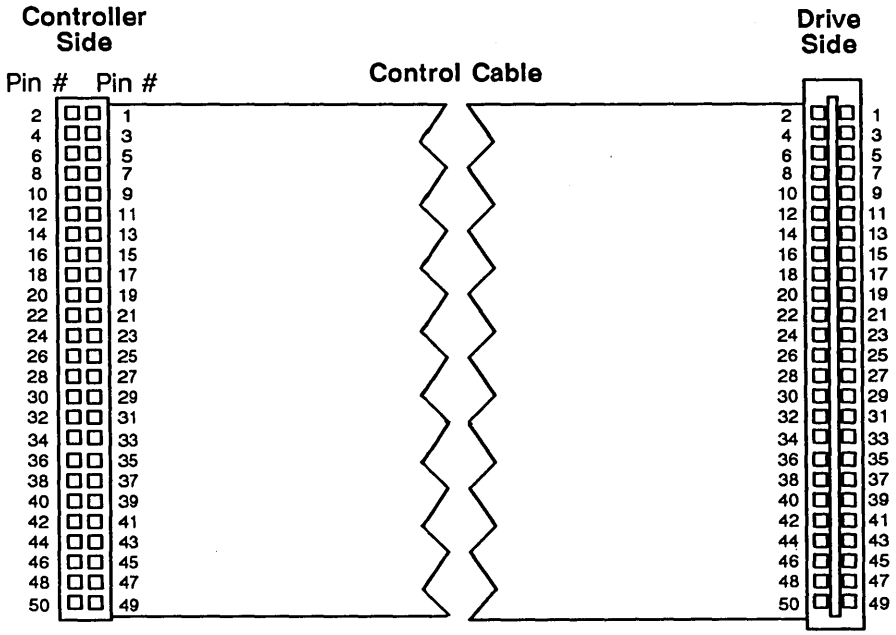


Figure 9-4. Tape Cartridge Drive Ribbon Cable Connectors

9.8 Environmental Conditions

Tables 9–4 and 9–5 list the environmental specifications for the tape drive.

Table 9–4. Tape Drive Environmental Specifications (Operating)

Characteristic	Specification
Temperature	5 to 45 °C (41 to 113 °F)
Temperature Gradient	1 °C (1.8 °F) maximum per minute 10 °C (18 °F) maximum per hour (noncondensing)
Wet Bulb Temperature	26 °C (79 °F) maximum
Relative Humidity	20 to 80%
Altitude	–200 to 15,000 feet above sea level
Vibration	0 to 63 Hz, 0.005 inch peak–to–peak, 63 to 500 Hz, 0.5 G peak
Shock	2.5 G peak (1/2 sine wave, 11–msec duration) on any axis)

Table 9–5. Tape Drive Environmental Specifications (Nonoperating, Unpackaged)

Characteristic	Specification
Temperature	–30 to 60 °C (–22 to 140 °F)
Temperature Gradient	30 °C (54 °F) maximum per hour (noncondensing)
Wet Bulb Temperature	26 °C (79 °F) maximum
Relative Humidity	10 to 90% (noncondensing)
Altitude	–200 to 50,000 feet above sea level
Vibration	0 to 17 Hz, 0.1 inch peak–to–peak, 17 to 500 Hz, 1.5 G peak
Shock	25 G peak (1/2 sine wave, 11–msec duration on any axis)

Chapter 10

Graphics Controllers

This chapter describes the specifications for the graphics controllers used in the DN3000 and DN4000 AT-compatible bus.

10.1 4-Plane Color Graphics Controller

The 4-plane color graphics controller has the following features:

- High-resolution 1024-pixel x 800-line x 4-plane display
- 16 simultaneous colors selectable from a palette of 4096
- Flicker-free, 60-Hz noninterlaced screen refresh
- Small physical size and low power requirements
- Dual-port, 512-KB image memory using high-density dynamic RAMs
- High-speed image and main memory BLTs facilitated by specialized gate arrays
- Support for the DN3000 6-MHz AT bus

10.1.1 Packaging Characteristics

The 4-plane color graphics controller is a standard AT-size printed circuit board, approximately 33.66 cm x 11.43 cm (13.25 inches x 4.5 inches). The board can be plugged into any AT-type slot on the motherboard. Figure 10-1 shows the color controller PCB.

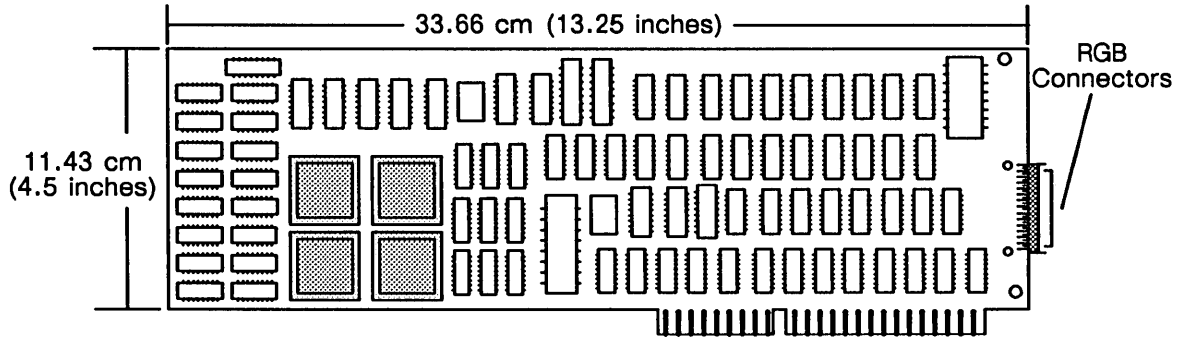


Figure 10–1. 4–Plane Color Graphics Controller PCB

10.1.2 Cabling

The color display cable carries monitor signals from the color graphics controller to the monitor. It is terminated at the monitor end with three BNC connectors (one for each of the RGB signals). The color monitor connects to the Red, Green, Blue (RGB) signals generated by the color graphics controller. Figure 10–2 shows the color display cable used with the 1024 x 800 x 4 color graphics controller.

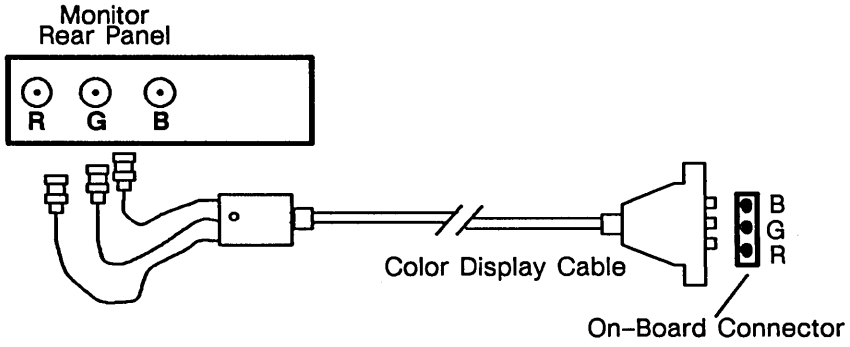


Figure 10–2. Color Display Cable

10.1.3 Voltage and Power Requirements

The following voltage is provided (via the motherboard) to the color graphics controller board:

+5.0 (± 0.25) Volts (at 3.0 A)

10.2 1280 x 1024 Monochrome Graphics Controllers

Two monochrome graphics controllers are available for the *Domain System*. The DN3000 controller (008157) is designed for use in a 6–MHz AT–bus environment; the DN4000 controller (010735) is designed for use in an 8–MHz AT–bus environment. Both controllers have the following features:

- High–resolution 1280–pixel x 1024–line display
- Flicker–free, 64–Hz noninterlaced screen refresh
- Low power requirements
- 256–KB image memory using high–density dynamic Dual–Ported Video RAMs
- High–speed image and main memory Block Transfers (BLT) facilitated by a specialized gate array

The major differences in the conrtrollers are an increase in clock speed for the DN4000 controller and the alteration of several logic elements to support the new clock speed. The remaining major specifications, including board layout and population, are unchanged.

10.2.1 Packaging Characteristics

The 1280 x 1024 monochrome graphics controllers are standard AT-size printed circuit boards, approximately 33.66 cm x 11.43 cm (13.25 inches x 4.5 inches). The boards can be plugged into any AT-type slot on the motherboard. Figure 10-3 shows the monochrome graphics controller PCBs.

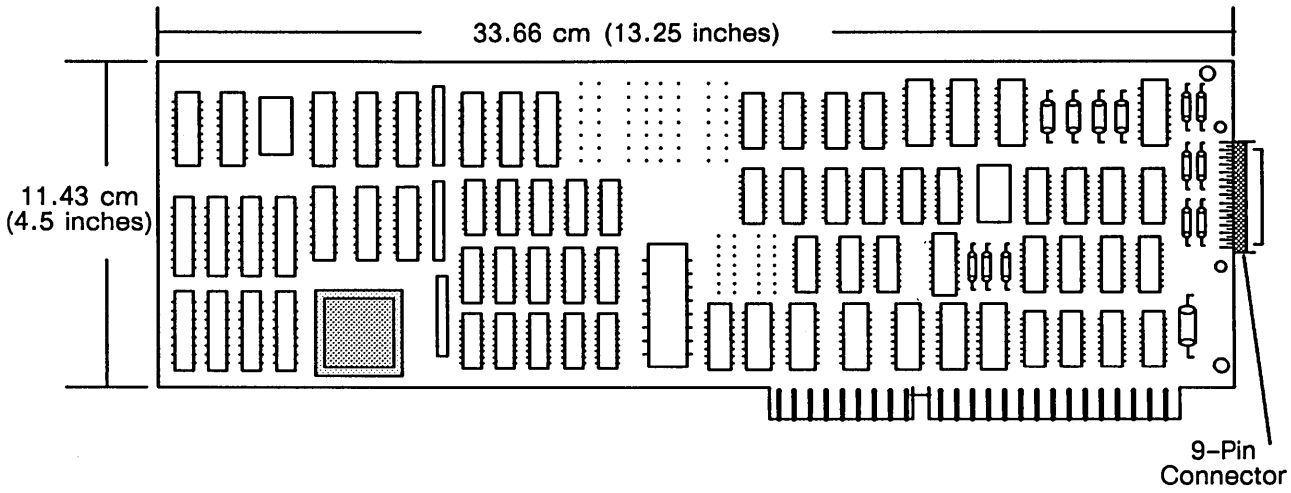


Figure 10-3. 1280 x 1024 Monochrome Graphics Controller PCB

10.2.2 Cabling

The monochrome graphics controller video and sync outputs are connected to the monitor via a twisted-pair shielded cable, which is terminated at the monitor. The cable attaches to the controller by a 9-pin, subminiature, D-shell connector.

Figure 10-4 shows the monochrome graphics controller cable.

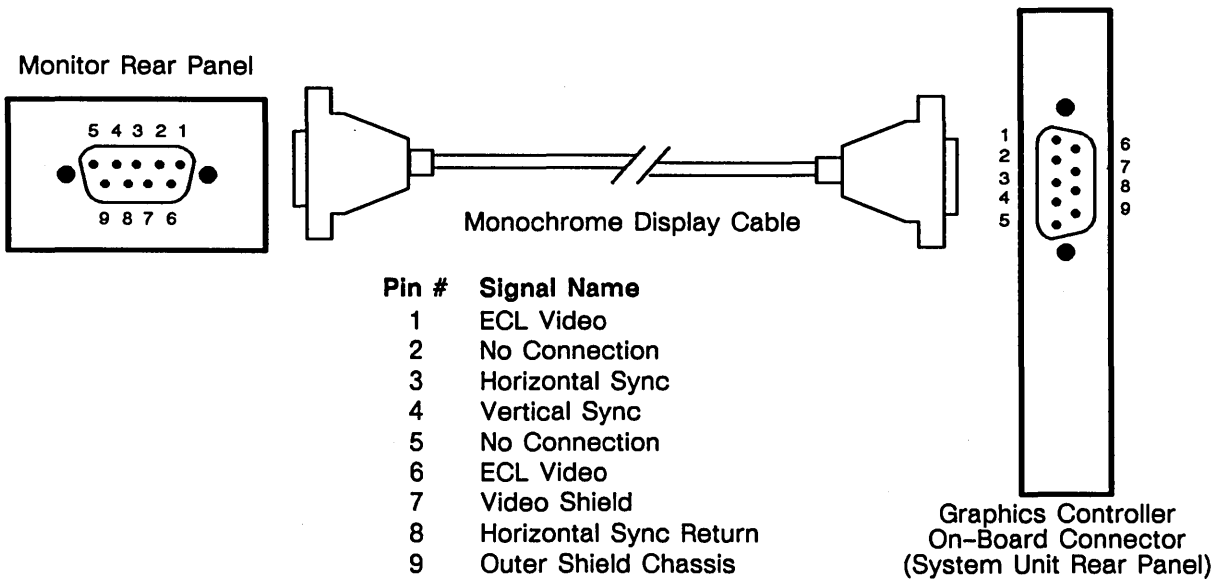


Figure 10–4. Monochrome Display Cable

10.2.3 Voltage and Power Requirements

The following voltages are provided (via the motherboard) to the monochrome graphics controller board:

+5.0 (± 0.25) Volts (at 2.2 A)

-5.0 (± 0.4) Volts (at 0.05 A)

10.3 8–Plane Color Graphics Controller

The 8-plane color graphics controller (010104) has the following features:

- High-resolution, 1024-pixel x 800-line x 8-plane display
- 256 simultaneous colors selectable from a palette of 16.7 million shades
- Flicker-free, 60-Hz noninterlaced screen refresh
- Small physical size and low power requirements
- Dual-port, 1-MB image memory using 64K x 4 dynamic RAMs
- High-speed image and main memory BLTs facilitated by specialized gate arrays
- Designed for use with the 6-MHz DN3000 AT bus or the 8-MHz DN4000 AT bus

The controller consists of the following functional blocks:

- Image Memory for storing a bit map of the image to be displayed
- Memory Data Path to provide registers, muxes, and logic to support bit BLT operations on the image memory
- Video Output Logic that drives the monitor with video signals that represent the bit map image
- Sync Generator to produce the timing signals necessary to generate the video output signals
- Bus Interface to connect the controller to the main CPU via the AT-compatible bus
- Control Logic to regulate the operation of the other functional blocks

10.3.1 8-Plane Differences

The 8-plane controller has been modeled after the DN3000 4-plane color display controller. The primary differences are as follows:

- Four additional planes of image memory
- Bus Interface designed for 8-MHz bus clock
- Device ID changed register to readback $0A
- ROP Register specifiers increased to 32 bits
- Moved Diagnostic memory request to previously unused address location
- Destination Plane Selection (D_PLANE) increased to 8 bits
- Added a second 82C55A
- Added a Miscellaneous Access register
- Added a second Miscellaneous Control register
- Source Plane Selection (S_PLANE) increased to 3 bits and moved to the added 82C55A
- Lookup Tables use combined RAM and triple 8-bit DAC's, changing table size to 256 x 24

10.3.2 Packaging Characteristics

The 8-plane color graphics controller is a standard AT-size printed circuit board, approximately 33.66 cm x 11.43 cm (13.25 inches x 4.5 inches). The board can be plugged into any AT-type slot on the motherboard. Figure 10-5 shows the color controller PCB.

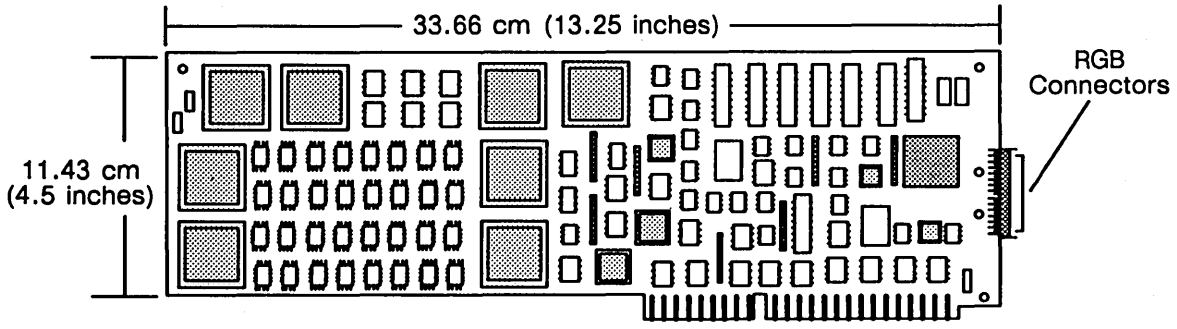


Figure 10-5. 8-Plane Color Graphics Controller PCB

10.3.3 Cabling

The color display cable carries monitor signals from the color graphics controller to the monitor. It is terminated at the monitor end with three BNC connectors (one for each of the RGB signals). The color monitor connects to the Red, Green, Blue (RGB) signals generated by the color graphics controller.

Figure 10–6 shows the color display cable used with the 8–plane color graphics controller.

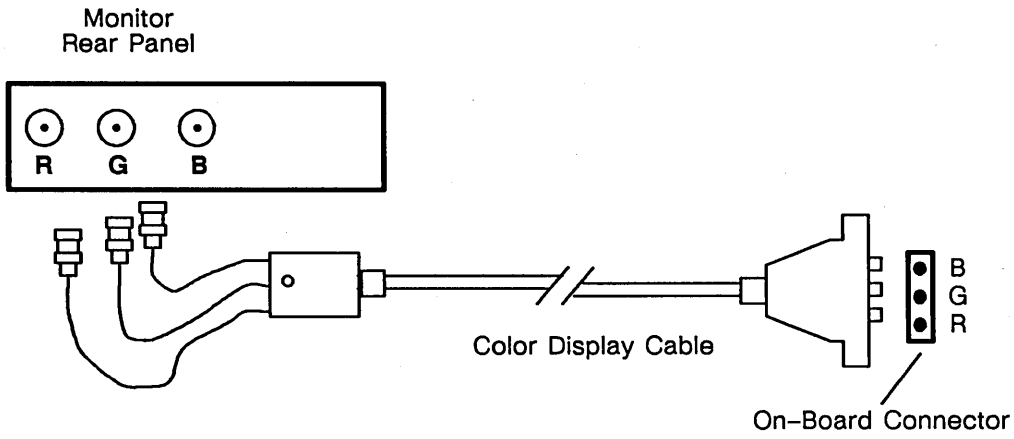


Figure 10–6. Color Display Cable

10.3.4 Voltage and Power Requirements

The following voltage is provided (via the motherboard) to the 8–plane color graphics controller board:

+5.0 (± 0.25) Volts (at 2.5 A typical)

10.4 Bus Interface

Refer to Chapter 2 of this manual for AT–compatible bus interface information. The main CPU controls the display board's operation through the AT–compatible bus interface. The controller is a slave device on the bus.

10.5 Cooling Requirements

The heat dissipated by the graphics controller is removed by forced air cooling. For proper cooling, the system fan must generate a suitable air flow across the board.

Chapter 11

Monitors

This chapter lists the specifications for the workstation monitors.

Figure 11–1 shows the 15–inch, high–resolution, 60–Hz, noninterlaced, 1024 x 800 bitmapped color monitor.

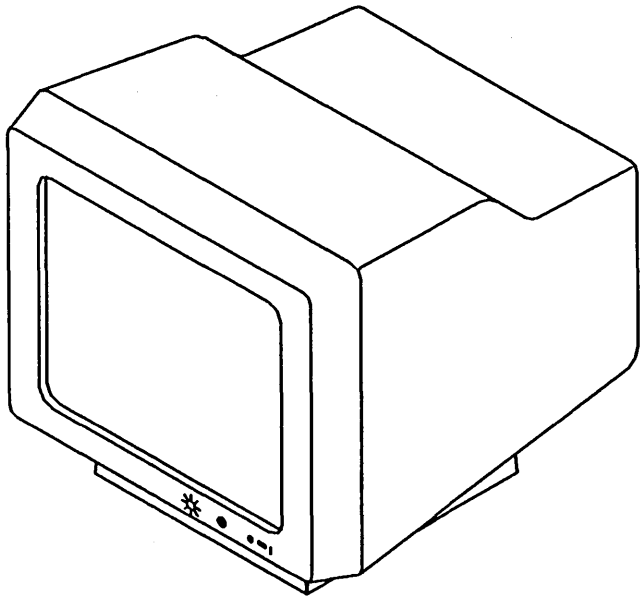


Figure 11–1. Domain System 15–Inch Color Monitor

Figure 11–2 shows the 19–inch, high–resolution, 60–Hz, noninterlaced, 1024 x 800 bitmapped color monitor.

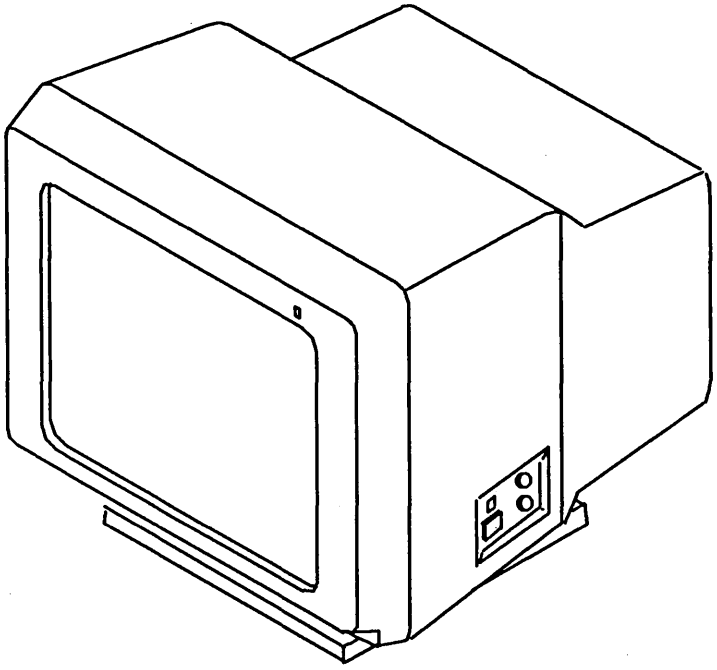


Figure 11–2. Domain System 19–Inch Color Monitor

Figure 11–3 shows the 19–inch, high–resolution, 60–Hz, noninterlaced, 1280 x 1024 bitmapped monochrome monitor.

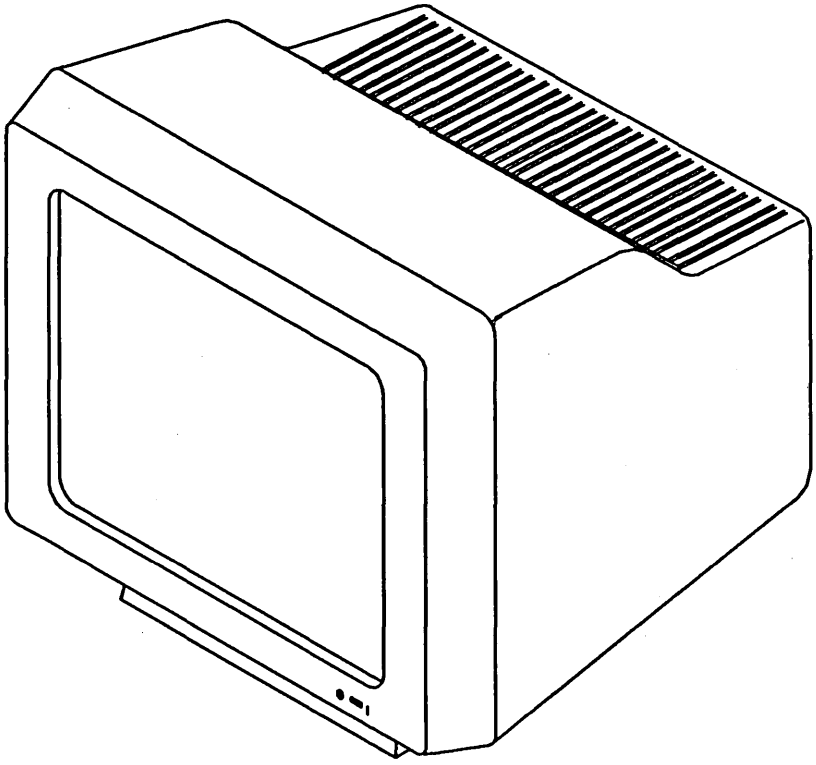


Figure 11–3. Domain System Monochrome Monitor

11.1 Color Monitor Specifications

Subsections 11.1.1 through 11.1.7 contain performance specifications for the 15-inch and 19-inch color monitors.

11.1.1 Video and Sync Signal Requirements

Three BNC receptacles (one for each R, G, and B connector) are used for video input at the rear of each color monitor. The synchronizing (SYNC) signal is a composite sync signal (horizontal and vertical sync mixed) that the color graphics controller provides on the Green signal line.

Table 11-1 lists the video and sync signal requirements.

Table 11-1. Video and Sync Signal Requirements

Item	Specification
Levels	0.5 to 1.5 V peak-to-peak plus sync (composite)
Polarity	RGB – Positive Sync – Negative
Impedence	Terminated – 75 ohms (± 2%) Unterminated – Greater than 10 kohms
Signal Waveform	EIA RS-343A-compatible

11.1.2 CRT Specifications

Table 11-2 lists the color monitor CRT specifications.

Table 11-2. Color Monitor CRT Specifications

Item	Specification	
	15-Inch Monitor	19-Inch Monitor
Size	16 inches (15-inch vertical measure)	20 inches (19-inch vertical measure)
Electron Gun	Precision in-line	Precision in-line
Convergence	Self-convergence	Self-convergence
Deflection Angle	90 degrees	90 degrees
Dot Trio Pitch	0.31 mm	0.32 mm
Phosphor	Medium persistence P22	Medium persistence P22
Surface	Anti-glare, high-contrast (A/R coat, tranmission 60% overall)	Anti-glare, high-contrast (A/R coat, tranmission 58% overall)
CRT Type	Matsushita 38JFG36X/B	Matsushita 48JFJ50X/B
Deflection Yoke	Matsushita Type SST	Matsushita Type SST

11.1.3 General Monitor Performance

The 15-inch and 19-inch color monitors must meet the performance specifications listed in Table 11-3.

Table 11-3. Color Monitor Performance Specifications

Item	Specification
Resolution	1024 x 800 (noninterlaced)
Scanning Frequency Range	Horizontal - 50.2 kHz (±500 Hz) Vertical - 47 to 80 Hz
Blanking Time	Horizontal - 4.713 µsec maximum Vertical - 828.83 µsec maximum (15-inch) 831 µsec maximum (19-inch)
Retrace Time	Horizontal - 3.713 µsec maximum Vertical - 600 µsec maximum
Video Amplifier:	
Bandwidth	±3 dB from 50 Hz to 70 MHz minimum
Pulse Rise and Fall Time	5 nanoseconds (max) measured from 10% to 90%
Differential Tilt	Not More than 3% on blanking waveforms
Video Polarity	Positive for Peak Luminance of the CRT
Video Gain	No perceptable difference at any brightness setting when a 15-nanosecond pixel is written adjacent to a 60-nanosecond bar
Intensity Modulation	No noticible change of intensity shall be present whether synchronous or asynchronous when viewed with the unaided eye at a distance of 457 mm
Degauss:	
Duration	Less than 15 seconds
Type	Automatic at power-on
X-Ray Radiation	Less than 0.5 MR/H

11.1.4 Signal Timing

The color monitors for Domain nodes utilize a composite Green signal. This signal includes the display signal for green and the composite synchronizing signal for both vertical and horizontal alignment. Within the composite sync signal, 842 horizontal periods occur for each vertical period. See Figure 11–4 and Table 11–4 for timing requirements of the various portions of the composite video signal.

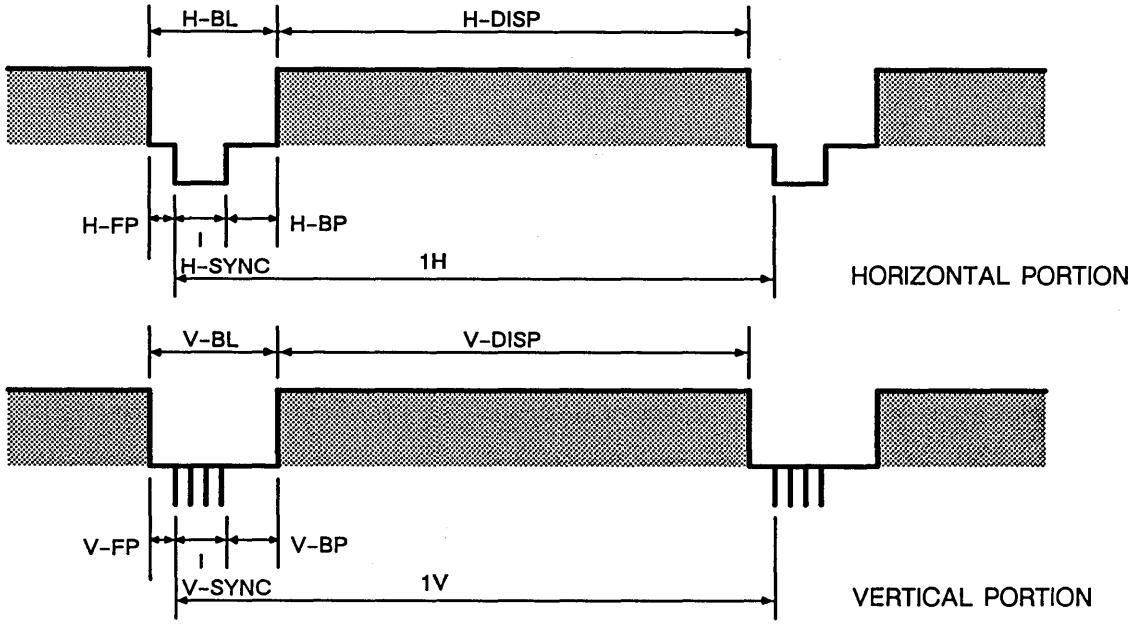


Figure 11–4. Signal Waveforms

Table 11–4. Color Monitor Timing, Frequency, and Duration

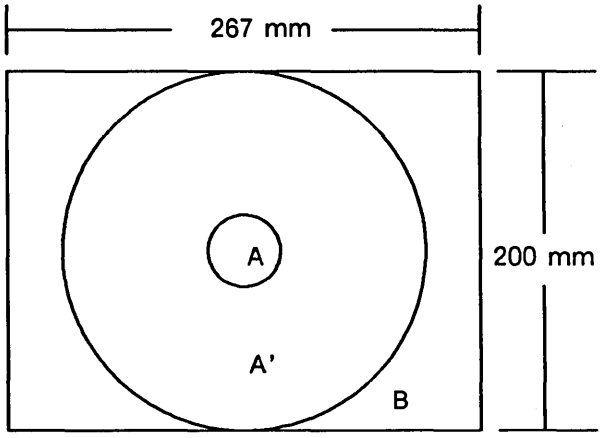
Axis	Item	Duration	Frequency
HORIZONTAL	Horizontal Frequency (1H)	19.794 µsec	50.519 kHz
	Horizontal Front Porch (H-FP)	0.942 µsec	N/A
	Horizontal Sync (H-Sync)	1.88 µsec	N/A
	Horizontal Back Porch (H-BP)	1.88 µsec	N/A
	Horizontal Blanking (H-BL)	4.71 µsec	N/A
	Horizontal Display Area (H-Disp)	15.084 µsec	N/A
VERTICAL	Vertical Frequency (1V)	16.67 msec	60.0 Hz
	Vertical Front Porch (V-FP)	79.176 µsec	N/A
	Vertical Sync (V-Sync)	79.176 µsec	N/A
	Vertical Back Porch (V-BP)	673.0 µsec	N/A
	Vertical Blanking (V-BL)	828.83 µsec (15-inch) 831 µsec (19-inch)	N/A
	Vertical Display Area (V-Disp)	15.841 msec (15-inch) 15.839 msec (19-inch)	N/A

11.1.5 Display Performance

15-Inch Color Monitor Convergence

Diameter of A circle is 25 mm.
Diameter of A' circle is 200 mm.
Area B is equal to the remaining area outside of circle A'.

Area A $\leq$ 0.15 mm maximum
Area A' $\leq$ 0.4 mm maximum
Area B $\leq$ 0.5 mm maximum

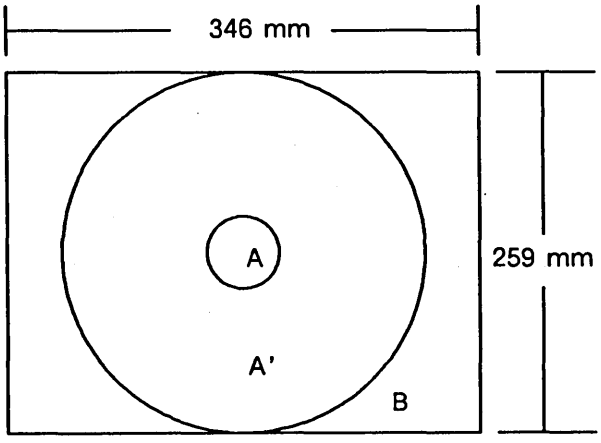


Terrestrial Magnetism
Vertical Field: Northern
Hemisphere Field: 0.5 Gauss
Horizontal Field: No Field

19-Inch Color Monitor Convergence

Diameter of A circle is 25 mm.
Diameter of A' circle is 259 mm.
Area B is equal to the remaining area outside of circle A'.

Area A $\leq$ 0.15 mm maximum
Area A' $\leq$ 0.4 mm maximum
Area B $\leq$ 0.5 mm maximum



Terrestrial Magnetism
Vertical Field: Northern
Hemisphere Field: 0.5 Gauss
Horizontal Field: No Field

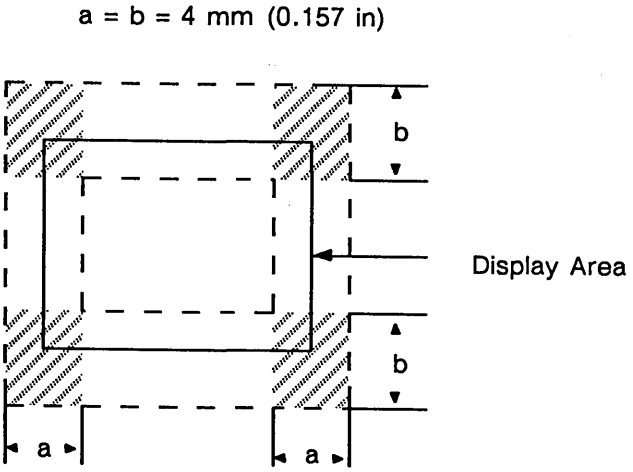
15-Inch and 19-Inch Color Monitor Linearity

Using a 1-inch pitch cross-hatch test signal, the maximum and minimum interval anywhere on the screen is calculated as follows:

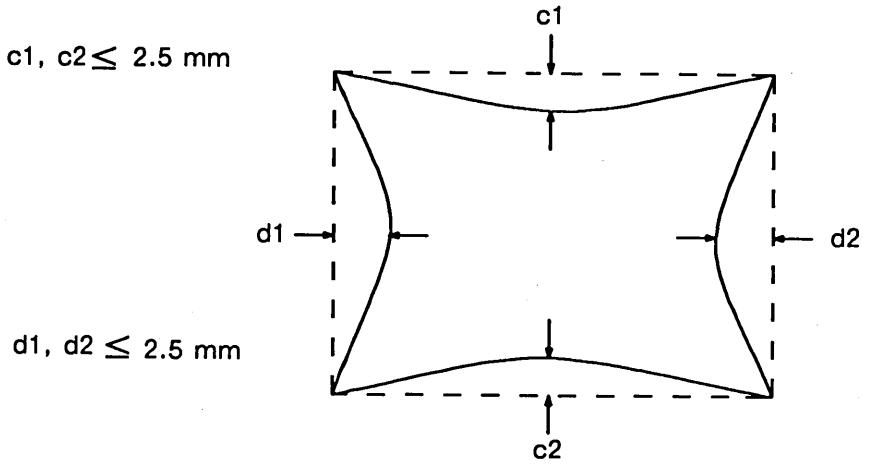
$$\frac{\text{MAXIMUM} - \text{MINIMUM}}{\text{MAXIMUM} + \text{MINIMUM}} \leq 5\% \text{ (horizontally and vertically)}$$

15-Inch Color Monitor Raster Distortion

Using the trapezoid and parallelogram test signal, the edge of the display image must be within the area indicated by the oblique line in the following illustration.

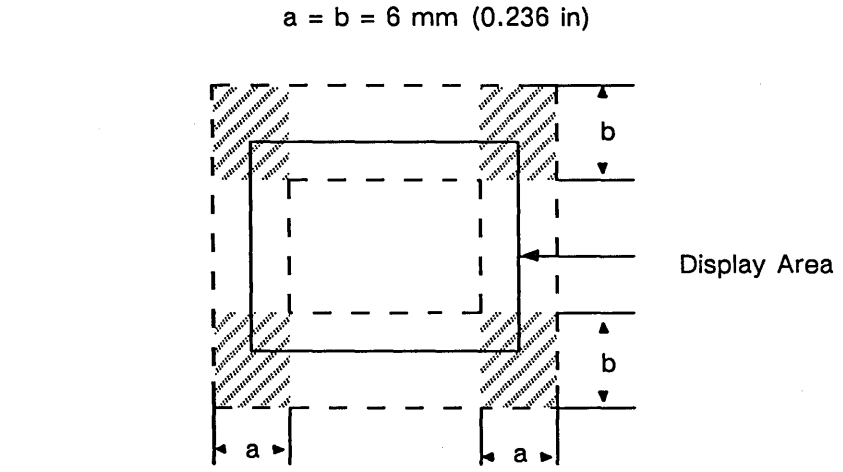


Using the pincushion test signal, the edge of the display image must be within the area indicated by the oblique line in the following illustration.

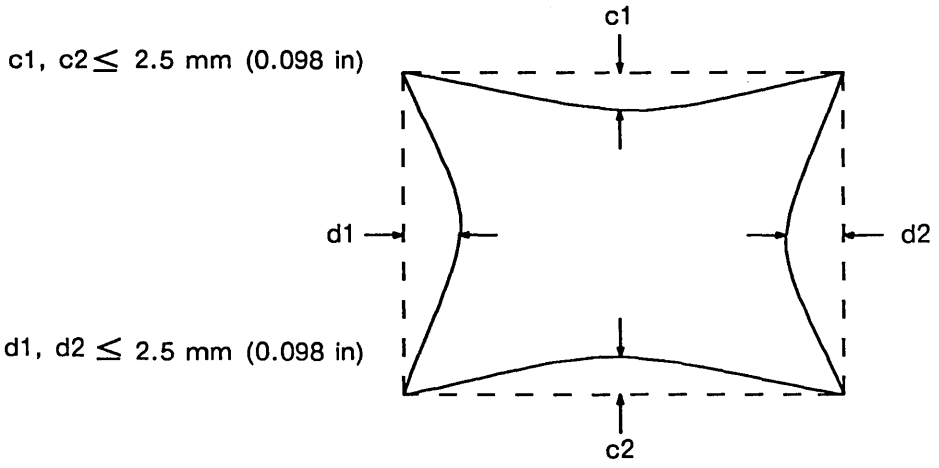


19–Inch Color Monitor Raster Distortion

Using the trapezoid and parallelogram test signal, the edge of the display image must be within the area indicated by the oblique line in the following illustration.



Using the pincushion test signal, the edge of the display image must be within the area indicated by the oblique line in the following illustration.



15–Inch Color Monitor Raster Size Regulation

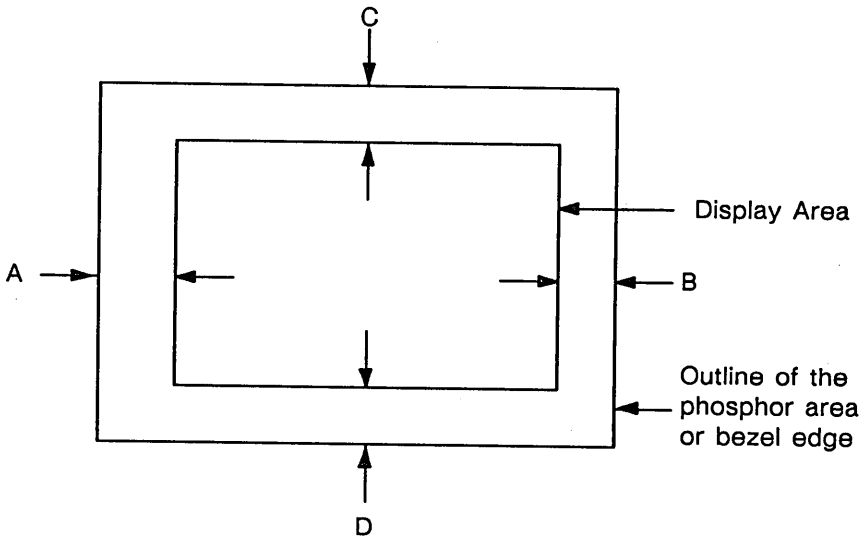
There must be less than 1.0% maximum raster dimension change with 0 to 100% APL (Average Picture Level) at a peak luminance of 12.5 FL on a white flat field with every available pixel location on.

19–Inch Color Monitor Raster Size Regulation

There must be less than 1.0% maximum raster dimension change with 0 to 100% APL (Average Picture Level) at a peak luminance of 11 FL on a white flat field with every available pixel location on.

15-Inch and 19-Inch Color Monitor Display Centering

The display must be centered on the CRT face within 6 mm horizontally. The measurement is done by taking a differential between A and B. The differential must not exceed 6 mm. The vertical display shall be centered on the CRT within 6 mm. The measurement is done by taking a differential between C and D. The yoke rotational error must not exceed 1 degree maximum.



15-Inch Color Monitor Available Brightness

Conditions:

1. Full white field of 100% duty cycle displayed, with a signal input amplitude of 714 millivolts from blanking level to reference white level.
2. Brightness control at center position.
3. Contrast control at maximum clockwise position.

The light output as measured at center screen must be 12.5 FL minimum and 25 FL maximum. No background raster is acceptable with the brightness control in the center position. When the contrast and brightness control is rotated to its maximum counterclockwise position, the light output must be no more than 5 FL. The minimum to maximum brightness ratio is calculated as follows:

$$\frac{\text{MAXIMUM BRIGHTNESS}}{\text{MINIMUM BRIGHTNESS}} \text{ equal to no less than 2.5 to 1}$$

Measured between the center and corners of the CRT, there must be no more than a 50% decrease in light output at any one corner.

19-Inch Color Monitor Available Brightness

Conditions:

1. Full white field of 100% duty cycle displayed, with a signal input amplitude of 714 millivolts from blanking level to reference white level.
2. Brightness control at center position.
3. Contrast control at maximum clockwise position.

The light output as measured at center screen must be 9 FL minimum and 14.5 FL maximum. No background raster is acceptable with the brightness control in the center position. When the contrast and brightness control is rotated to its maximum counterclockwise position, the light output must be no more than 5 FL. The minimum to maximum brightness ratio is calculated as follows:

$$\frac{\text{MAXIMUM BRIGHTNESS}}{\text{MINIMUM BRIGHTNESS}} \text{ equal to no less than 2.5 to 1}$$

Measured between the center and corners of the CRT, there must be no more than a 50% decrease in light output at any one corner.

15-Inch and 19-Inch Color Monitor Color Temperature

The color temperature must be adjusted to 9300° C + 27 MPCD as represented by the X and Y chromaticity coordinates of X = 0.281 and Y = 0.311 (± 5%). The reference instrument is a Color Analyzer II by Minolta. All controls used to set color tracking and cutoff must be factory sealed.

15-Inch and 19-Inch Color Monitor Tracking

From maximum brightness output to minimum brightness output, no single color should achieve dominance. If questionable, the measurement must be done at 5 FL of brightness and be within the range for the X and Y coordinates for 9300° C (± 7%).

15-Inch Color Monitor Display Area

The display area of the monitor should be 267 mm x 200 mm (± 5 mm) at rated timing.

19-Inch Color Monitor Display Area

The display area of the monitor should be 346 mm x 259 mm (± 5 mm) at rated timing.

15-Inch and 19-Inch Color Monitor Aspect Ratio

The display must achieve an aspect ratio of 4:3.

15-Inch and 19-Inch Color Monitor Emission Warm-Up Time

The emission warm-up time must be less than 20 seconds.

15-Inch and 19-Inch Color Monitor Drift

The monitor must operate over the specified temperature range (0° C to 50° C) without losing synchronization or any visible change in light output. No manual adjustments should be necessary over the specified temperature range.

11.1.6 Color Monitor Power Requirements

This subsection lists the power requirements for the color monitors. The ac power cord mates with an IEC grounding type 3-pin male connector on the rear panel of the monitor.

Table 11–5 lists the color monitor power specifications.

Table 11–5. Color Monitor Power Specifications

Item	Specification	
	15-Inch	19-Inch
Input Voltage	90 to 132 V ac or 180 to 264 V ac (switch-selectable)	90 to 132 V ac or 180 to 264 V ac (switch-selectable)
Frequency	50 or 60 Hz (±3) @ 120 V 50 (±1) Hz @ 240 V	50 or 60 Hz (±3) @ 120 V 50 (±1) Hz @ 240 V
Power Consumption	Less than 200 watts	Less than 200 watts
Power Surge Current	Power-On - Less than 50 A Peak @ 120 V ac	Power-On - Less than 50 A Peak @ 120 V ac
Input Current	2 A maximum @ 120 V 1 A maximum @ 240 V	2 A maximum @ 120 V 1.25 A maximum @ 240 V

11.1.7 Color Monitor Display Cable

The display cable connects the monitor to the graphics controller board in the system unit. Figure 11–5 shows the color display cable.

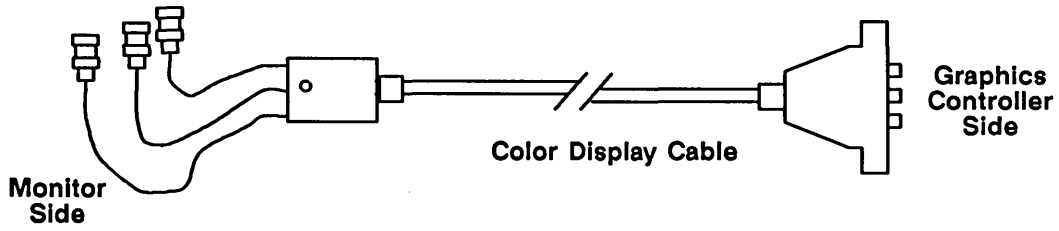


Figure 11–5. Color Display Cable

11.2 Monochrome Monitor Specifications

Table 11–6 lists the signal specifications for the 19–inch monochrome monitor.

Table 11–6. Monochrome Monitor Signal Specifications

Item	Video Signal	Vertical Signal	Horizontal Signal
Input Level	ECL Balanced	TTL	TTL
Polarity	Positive	Positive	Positive
Impedence	100 ohms (±5%)	200 ohms (±5%)	200 ohms (±5%)
Interconnection: Twisted pair, 100 ohms impedance, shielded			

11.2.1 CRT Specifications

The monochrome monitor's CRT conforms to the specifications in Table 11–7.

Table 11–7. Monochrome Monitor CRT Specifications

Item	Specification
Size	19 inches
Electron Gun	Low-voltage focus
Neck Diameter	28 mm
Deflection Angle	114 degrees
Faceplate Transmission	44%
Phosphor	PC–104 or equivalent
Surface Treatment	Anti-glare specular glass 60 degree large aperture = 50 to 60

11.2.2 General Monitor Performance

The monochrome monitor performs within the specifications listed in Table 11-8.

Table 11-8. Monochrome Monitor Performance Specifications

Item	Specification
Resolution	1280 x 1024 noninterlaced
Active Video Time	Horizontal - 10.857 μsec Vertical - 15.009 milliseconds
Blanking Time	Horizontal - 3.8 μsec Vertical - 616 μsec
Front Porch	Horizontal - 407 nanoseconds Vertical - 58.6 μsec
Back Porch	Horizontal - 1.9 μsec Vertical - 498 μsec
Sync Pulse	Horizontal - 1.49 μsec Vertical - 58.6 μ sec
Pixel Time	8.47 nanoseconds
Maximum Light Output	30 (± 5) FLB
Minimum Light Output	Less than 5 FLB with brightnee control set full CCW
Contrast Ratio	5:1 with 100 FC ambient perpendicular to work surface

11.2.3 Display Performance

This subsection lists the various display performance specifications.

Raster Size

The Horizontal Raster size is 349 mm (± 1%). The Vertical Raster size is 279 mm (± 1%).

Raster Size Regulation

The Raster Size Regulation is less than a 1% change between 5 FLB and 30 FLB

Horizontal and Vertical Linearity

The height or width of any adjacent cell of a cross-hatch pattern must be within 6% to 10% of that of any cell on the active screen.

Geometry

When the display size is adjusted to 356 x 279 mm, all pincushion, barrel, keystoning, and distortions should fall within a 4 mm wide margin centered at an ideal rectangle.

Drift

The monitor operates over the specified temperature range without loss of sync. No manual adjustments are necessary over the specified temperature range. All specifications will be maintained over the specified temperature range, after a 20-minute, warm-up period.

Emission Warm-Up Time

The emission warm-up time is 20 seconds.

Dot Displacement

No visible dot displacement (jitter or swim) is allowed, as viewed at a distance of 457 mm in normal office lighting.

Intensity Modulation and Velocity Modulation

No discernible change of intensity shall be present whether synchronous or asynchronous, as viewed with the unaided eye at a distance equal to 457 mm.

Brightness Uniformity

Brightness uniformity should not exceed a 30% change anywhere within the active raster.

11.2.4 Monochrome Monitor Power Requirements

This subsection list the power requirements for the monochrome monitor. The ac power cord mates with an IEC grounding type 3-pin male connector on the rear panel of the monitor.

Table 11-9 lists the monochrome monitor power specifications.

Table 11-9. Monochrome Monitor Power Specifications

Item	Specification
Input Voltage	90 to 132 V ac or 180 to 264 V ac (switch-selectable)
Frequency	50 or 60 Hz (±3) @ 120 V 50 (±1) Hz @ 240 V
Power Consumption	Less than 100 watts
Power Surge Current	Power-On - Less than 50 A peak @ 120 V ac
Input Current	1.5 A maximum @ 120 V 0.75 A maximum @ 240 V

11.2.5 Monochrome Monitor Display Cable

The display cable connects the monitor to the graphics controller board in the system unit. Figure 11-6 shows the monochrome display cable.

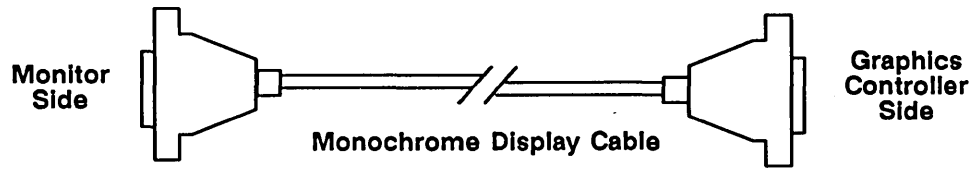


Figure 11-6. Monochrome Display Cable

11.3 Environmental Specifications

Table 11–10 lists the environmental specifications for all of the monitors.

Table 11–10. Monitor Environmental Specifications

Item	Specification
Temperature	Operating = 0 to 40 degrees C Nonoperating = –20 to 60 degrees C
Humidity	5% to 90% noncondensing
Altitude	Operating = 3000 meters (10,000 feet) Nonoperating = 12,000 meters (40,000 feet)

Chapter 12

Keyboard

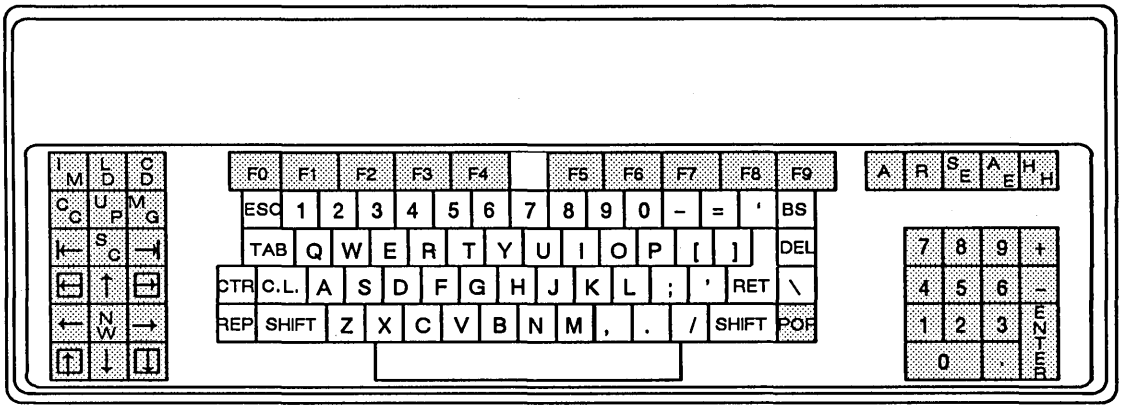
The *Domain System* keyboard generates scan codes from one of two sets of character codes, performs power-up and operator requested self-diagnostics, and controls and reports the status of the CAPS LOCK LED. It also coordinates communications between the CPU, the keyboard, and the pointing device, and controls the on-board speaker. By using two sets of character codes, the keyboard is compatible with all Domain nodes. One set of character codes uses ASCII-like code definitions (as with earlier Domain keyboards); the other set of codes uses keystate definitions.

The keystate codes tell the CPU when each key is pressed and released; they do not make interpretations about the positions of the state keys (CTRL, SHIFT, etc.) relative in time to the position of the other keys. Another feature of the keyboard is that it it is powered from a voltage source of either +5 V dc or +8.5 V dc, again allowing compatiblity with all Domain nodes.

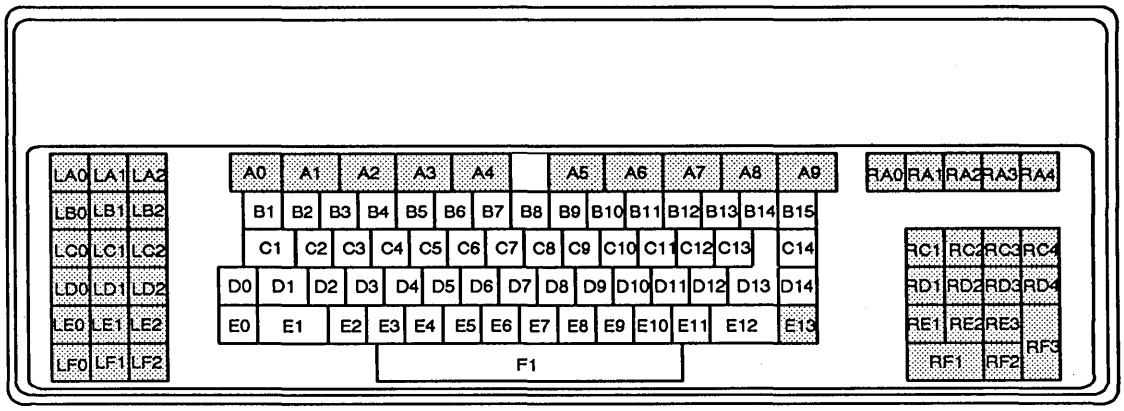
The keyboard is a microprocessor controlled device, capable of receiving commands from and sending commands to the CPU. These commands define the mode of operation for the keyboard and determine how data is sent.

12.1 Keyboard Layout

The Model II Keyboard includes the standard alphabetic, numeric, and symbol keys as well as 48 programmable function keys. The function keys are divided into three groups: left, top, and right. The right function keys are broken down further to include a numeric keypad. Figure 12–1 illustrates the keyboard layout. The function keys are shaded.



ACTUAL KEYCAPS



KEY NUMBERS

Figure 12–1. Keyboard Layout

12.2 Keyboard Character Codes

Tables 12–1 and 12–2 list the character codes sent by the Interface Module to the CPU. The ASCII mode is the default.

Table 12-1. ASCII Key Legends and Coding

Key Number	Keycap Legend	Unshifted Code	Shifted Code	Control Code	Caps Lock Code	Up Trans Code	Auto Repeat
LA0	INS/MARK	81	91	81	81	A1	No
LA1	LINE DEL	82	92	82	82	A2	No
LA2	CHAR DEL	83	93	83	83	A3	Yes
A0	F0	1C	5C	7C	1C	BC	No
A1	F1	C0	D0	F0	C0	E0	No
A2	F2	C1	D1	F1	C1	E1	No
A3	F3	C2	D2	F2	C2	E2	No
A4	F4	C3	D3	F3	C3	E3	No
A5	F5	C4	D4	F4	C4	E4	No
A6	F6	C5	D5	F5	C5	E5	No
A7	F7	C6	D6	F6	C6	E6	No
A8	F8	C7	D7	F7	C7	E7	No
A9	F9	1F	2F	3F	1F	BD	No
RA0	AGAIN	CD	E9	CD	CD	ED	No
RA1	READ	CE	EA	CE	CE	EE	No
RA2	SAVE/EDIT	CF	EB	CF	CF	EF	No
RA3	ABORT/EXIT	DD	EC	DD	DD	FD	No
RA4	HELP/HOLD	B3	B7	B3	B3	BB	No
LB0	CUT/COPY	B0	B4	B0	B0	B8	No
LB1	UNDO/PASTE	B1	B5	B1	B1	B9	No
LB2	MOVE/GROW	B2	B6	B2	B2	BA	No
B1	ESC	1B	1B	–	1B	–	No
B2	! 1	31	21	–	31	–	No
B3	@ 2	32	40	–	32	–	No
B4	# 3	33	23	–	33	–	No
B5	$ 4	34	24	–	34	–	No
B6	% 5	35	25	–	35	–	No
B7	^ 6	36	5E	–	36	–	No
B8	& 7	37	26	–	37	–	No
B9	* 8	38	2A	–	38	–	No
B10	(9	39	28	–	39	–	No
B11	) 0	30	29	–	30	–	No
B12	_ –	2D	5F	–	2D	–	Yes
B13	+ =	3D	2B	–	3D	–	Yes
B14	~ `	60	7E	1E	60	–	No
B15	BACK SPACE	DE	DE	–	DE	–	Yes
LC0	|←	84	94	84	84	A4	No
LC1	SHELL/CMD	85	95	85	85	A5	No
LC2	→|	86	96	86	86	A6	No
C1	TAB	CA	DA	FA	CA	–	No
C2	Q	71	51	11	51	–	No
C3	W	77	57	17	57	–	No
C4	E	65	45	05	45	–	No
C5	R	72	52	12	52	–	No
C6	T	74	54	14	54	–	No
C7	Y	79	59	19	59	–	No
C8	U	75	55	15	55	–	No
C9	I	69	49	09	49	–	No
C10	O	6F	4F	0F	4F	–	No
C11	P	70	50	10	50	–	No
C12	{ [	7B	5B	1B	7B	–	No
C13	}]	7D	5D	1D	7D	–	No
C14	DELETE	7F	7F	–	7F	–	Yes

(Continued)

Table 12-1. ASCII Key Legends and Coding (Cont.)

Key Number	Keycap Legend	Unshifted Code	Shifted Code	Control Code	Caps Lock Code	Up Trans Code	Auto Repeat
RC1	7	FE_37	FE_26	–	FE_37	–	No
RC2	8	FE_38	FE_2A	–	FE_38	–	No
RC3	9	FE_39	FE_28	–	FE_39	–	No
RC4	+	FE_2B	FE_3D	–	FE_2B	–	No
LD0	[←]	87	97	87	87	A7	No
LD1	↑	88	98	88	88	A8	Yes
LD2	[→]	89	99	89	89	A9	No
D0	CTRL	Control Key					
D1	CAPS LOCK	Capital Letters Lock Key			41		
D2	A	61	41	01	41	–	No
D3	S	73	53	13	53	–	No
D4	D	64	44	04	44	–	No
D5	F	66	46	06	46	–	No
D6	G	67	47	07	47	–	No
D7	H	68	48	08	48	–	No
D8	J	6A	4A	0A	4A	–	No
D9	K	6B	4B	0B	4B	–	No
D10	L	6C	4C	0C	4C	–	No
D11	: ;	3B	3A	FB	3B	–	No
D12	" '	27	22	F8	27	–	No
D13	RETURN	CB	DB	–	CB	–	No
D14	| \	C8	C9	–	C8	–	No
RD1	4	FE_34	FE_24	–	FE_34	–	No
RD2	5	FE_35	FE_25	–	FE_35	–	No
RD3	6	FE_36	FE_5E	–	FE_36	–	No
RD4	–	FE_2D	FE_5F	–	FE_2D	–	No
LE0	←	8A	9A	9A	9A	AA	Yes
LE1	NEXT WINDOW	8B	9B	8B	8B	AB	No
LE2	→	8C	9C	8C	8C	AC	Yes
E0	REPEAT	Repeat Key					
E1	SHIFT	Shift Key					
E2	Z	7A	5A	1A	5A	–	No
E3	X	78	58	18	58	–	No
E4	C	63	43	03	43	–	No
E5	V	76	56	16	56	–	No
E6	B	62	42	02	42	–	No
E7	N	6E	4E	0E	4E	–	No
E8	M	6D	4D	0D	4D	–	No
E9	< ,	2C	3C		2C	–	No
E10	> .	2E	3E		2E	–	Yes
E11	? /	CC	DC	FC	CC	–	No
E12	SHIFT	–	Shift Key	–	–	–	–
E13	POP	80	90	80	80	A0	No
RE1	1	FE_31	FE_21	–	FE_31	–	No
RE2	2	FE_32	FE_40	–	FE_32	–	No
RE3	3	FE_33	FE_23	–	FE_33	–	No
LF0	[↑]	8D	9D	8D	8D	AD	No
LF1	↓	8E	9E	8E	8E	AE	Yes
LF2	[↓]	8F	9F	8F	8F	AF	No
F1	(space bar)	20	20	20	20	–	Yes
RF1	0	FE_30	FE_29	–	FE_30	–	No
RF2	.	FE_2E	FE_2E	–	FE_2E	–	No
RF3	ENTER	FE_CB	FE_DB	–	FE_CB	–	No

The following list applies to Table 12–1:

- Keys that are specified to auto–repeat default to repeat the down transition only at 33 milliseconds (+/– 3 milliseconds) after an initial delay of 500 milliseconds (+/– 50 milliseconds). The repeat rate and delay can be reprogrammed via software.
- All keys are subject to the repeat key. They repeat the down transition at the programmed rate with no initial delay.
- All keys exhibit N–key rollover for a minimum of six simultaneous key depressions.
- The up transitions are not affected by the SHIFT, CTRL, or CAPS LOCK keys.
- The keyboard buffers at least 16 bytes of data. When all 16 positions are used, further processing of data is inhibited until a new position becomes available.
- The CAPS LOCK LED lights during down transitions of the key (if it was previously off), and goes off during up transitions (if it was previously on).

The following list applies to Table 12–2:

- The repeat function is handled by the keyboard by transmitting a 7F (hexadecimal) when any key (except CAPS LOCK) has been pressed for longer than the repeat rate time. The repeat rate time is programmed by the Set Repeat Rate command and defaults to 33 milliseconds (+/– 3 milliseconds).
- All keys (except CAPS LOCK) are subject to the repeat key. They repeat the down transition at the programmed rate with no initial delay. All repeat functions are handled by the keyboard and the host system.
- All keys exhibit N–key rollover for a minimum of six simultaneous key depressions.
- No key transition is affected or modified by any other key state.
- The keyboard buffers at least 16 bytes of data. When all 16 positions are used, further processing of data is inhibited until a new position becomes available.
- The CAPS LOCK key transmits the On/Off transition information according to the state of the LED. When the LED comes on, a 7E (hexadecimal) is transmitted; when the LED goes off, an FE (hexadecimal) is transmitted. The LED comes on during down transitions of the key when it was previously off, and goes off during up transitions when it was previously on.

Table 12–2. Keystate Mode Key Legends and Coding

Key Number	Keycap Legend	Down Transition Code	Up Transition Code
LA0	INS/MARK	01	81
LA1	LINE DEL	02	82
LA2	CHAR DEL	03	83
A0	F0	04	84
A1	F1	05	85
A2	F2	06	86
A3	F3	07	87
A4	F4	08	88
A5	F5	09	89
A6	F6	0A	8A
A7	F7	0B	8B
A8	F8	0C	8C
A9	F9	0D	8D
RA0	AGAIN	0E	8E
RA1	READ	0F	8F
RA2	SAVE/EDIT	10	90
RA3	ABORT/EXIT	11	91
RA4	HELP/HOLD	12	92
LB0	CUT/COPY	13	93
LB1	UNDO/PASTE	14	94
LB2	MOVE/GROW	15	95
B1	ESC	17	97
B2	! 1	18	98
B3	@ 2	19	99
B4	# 3	1A	9A
B5	$ 4	1B	9B
B6	% 5	1C	9C
B7	^ 6	1D	9D
B8	& 7	1E	9E
B9	* 8	1F	9F
B10	(9	20	A0
B11	) 0	21	A1
B12	_ -	22	A2
B13	+ =	23	A3
B14	~ `	24	A4
B15	BACK SPACE	25	A5
LC0	|←	27	A7
LC1	SHELL/CMD	28	A8
LC2	→|	29	A9
C1	TAB	2C	AC
C2	Q	2D	AD
C3	W	2E	AE
C4	E	2F	AF
C5	R	30	B0
C6	T	31	B1
C7	Y	32	B2
C8	U	33	B3
C9	I	34	B4
C10	O	35	B5
C11	P	36	B6
C12	{ [	37	B7
C13	}]	38	B8
C14	DELETE	3A	BA
RC1	7	3C	BC

(Continued)

Table 12–2. Keystate Mode Key Legends and Coding (Cont.)

Key Number	Keycap Legend	Down Transition Code	Up Transition Code
RC2	8	3D	BD
RC3	9	3E	BE
RC4	+	3F	BF
LD0	[←]	40	C0
LD1	↑	41	C1
LD2	[→]	42	C2
D0	CTRL	43	C3
D1	CAPS LOCK	CAPITOL LETTERS	LOCK KEY
D2	A	46	C6
D3	S	47	C7
D4	D	48	C8
D5	F	49	C9
D6	G	4A	CA
D7	H	4B	CB
D8	J	4C	CC
D9	K	4D	CD
D10	L	4E	CE
D11	: ;	4F	CF
D12	" '	50	D0
D13	RETURN	52	D2
D14	| \	53	D3
RD1	4	55	D5
RD2	5	56	D6
RD3	6	57	D7
RD4	-	58	D8
LE0	←	59	D9
LE1	NEXT WINDOW	5A	DA
LE2	→	5B	DB
E0	REPEAT	5D	DD
E1	SHIFT	5E	DE
E2	Z	60	E0
E3	X	61	E1
E4	C	62	E2
E5	V	63	E3
E6	B	64	E4
E7	N	65	E5
E8	M	66	E6
E9	< ,	67	E7
E10	> .	68	E8
E11	? /	69	E9
E12	SHIFT	6A	EA
E13	POP	6C	EC
RE1	1	6E	EE
RE2	2	6F	EF
RE3	3	70	F0
LF0	[↑]	72	F2
LF1	↓	73	F3
LF2	[↓]	74	F4
F1	(space bar)	76	F6
RF1	0	79	F9
RF2	.	7B	FB
RF3	ENTER	7C	FC
CAPS LOCK LED		7E (ON)	FE (OFF)

12.3 Keyboard Interface

There are two external interfaces associated with the keyboard, one interface with the CPU and a second with the cursor pointing device. Figure 12–2 shows the connector locations on the rear of the keyboard.

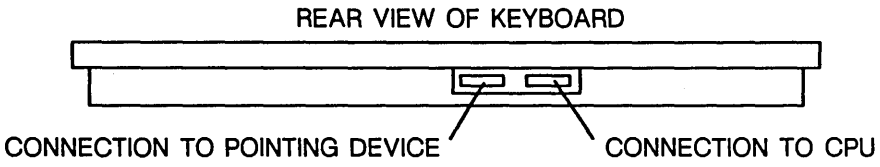
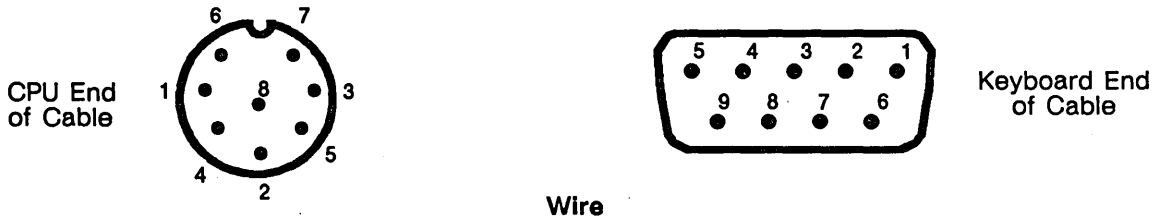


Figure 12–2. Keyboard Connections

12.3.1 CPU Connection

The cable connecting the keyboard to the CPU features a connector at each end. The connector at the CPU end is an 8-pin male DIN type, and the connector at the keyboard end is a 9-pin, female, D-sub-miniature type. Both cable connectors are illustrated in Figure 12–3.



CPU Connector			Wire Color	Keyboard Connector		
1	–	+8.5 V dc	Red	2	–	+8.5 V dc Series 3000 +12 V dc Series 4000
2	–	Data to CPU (TXD)	Yellow	4	–	Data to CPU (TXD)
3	–	Logic Ground	Green	6	–	Logic Ground
4	–	RESET	Orange	3	–	RESET
5	–	Data to Keyboard (RXD)	Gray	5	–	Data to Keyboard (RXD)
6	–	Not used		1	–	Not used
7	–	Logic Ground	Blue	7	–	Logic Ground
8	–	Not used		8	–	Not used
SHIELD	–	Chassis Ground		SHIELD	–	Chassis Ground
				9	–	Not used

Figure 12–3. Keyboard Cable Connectors

In the Series 3000, +8.5 V dc is supplied by the CPU and regulated to +5 V dc by the keyboard's internal voltage regulator. In the Series 4000, +12 V dc is supplied by the CPU and regulated to +5 V dc by the keyboard's internal voltage regulator.

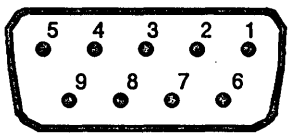
RESET* is a signal sourced by the CPU. The keyboard's scanning hardware may not drive this line. A low TTL voltage on RESET* will reset the keyboard.

KBD_TXD and KBD_RXD are serial data to and from (respectively) the CPU in the form of a 1200-baud asynchronous, full-duplex, communications link that is formatted as one start bit, eight data bits, one parity bit (even), and one stop bit. Mark = high TTL voltage and space = low TTL voltage.

Chassis ground must be kept electrically isolated from logic ground.

12.3.2 Pointing Device Connection

The mouse connector at the keyboard is a 9-pin, female, D-subminiature type (see Figure 12-4).



Pin	-	Signal
1	-	+5 V
2	-	YB
3	-	YA
4	-	XB
5	-	XA
6	-	Logic Ground
7	-	SWM (middle switch)
8	-	SWR (right switch)
9	-	SWL (left switch)
SHIELD	-	Chassis Ground

Figure 12-4. Pointing Device Connector (at Keyboard)

The keyboard responds to either quadrature or serial signals. The X and Y quadrature clock signals (XA, XB, YA, YB) and SWM, SWR, and SWL (signals from the middle, right, and left switches of the pointing device) are generated by such pointing devices as are defined in Chapter 13.

TX is serial data from the keyboard in the form of a 1200-baud asynchronous communications link that is formatted as one start bit (logic Zero, > 2.0 V), eight data bits, one parity bit (even), and one stop bit (logic One, < 0.8 V).

Chassis ground must be kept electrically isolated from logic ground.

Chapter 13 provides more information about the pointing device interface.

12.4 Keyboard Specifications

This section details the electrical and environmental specifications for the Domain Low-Profile Keyboard Model II.

12.4.1 Electrical Specifications

The electrical specifications for the Model II Low-Profile keyboard are as follows:

+ 7.9 volts to + 13 volts @ 600 mA dc and not to exceed 5.50 W maximum.

Maximum voltage cannot be applied at maximum current level to maintain maximum power level.

NOTICE: For measurements taken at keyboard connector, the current includes 300 mA for keyboard and 300 mA for pointing device.

12.4.2 Environmental Specifications

The environmental specifications for the keyboard are outlined in Table 12-3.

Table 12-3. Keyboard Environmental Specifications

Item	Specification
Ambient Room Temperature	15°C (59° F) to 32°C (90°F) operating -40°C nonoperating
Relative Humidity	20% to 80% operating 5% to 95% nonoperating
Altitude	0 to 2.44 km (8000 ft) operating 0 to 9.1 km (30,000 ft) nonoperating

Chapter 13

Pointing Devices

The standard pointing device for the *Domain System* is a quadrature mouse. By moving the mouse on your desktop, you manipulate the cursor on the display screen. In addition, switches on the top of the mouse serve as function keys similar to the function keys on the keyboard. This chapter describes how the cursor control and switch data is transferred from a pointing device to the CPU.

Pointing devices operate in one of two modes, absolute or relative. They also transmit data in one of two formats, quadrature or serial. A quadrature mouse transmits data in relative mode only; a serial device is capable of transmitting data in both modes. The mode of operation establishes how movements of the pointing device effect the position of the cursor on the display screen. In absolute mode, the pointing device surface emulates the screen, and cursor movements always begin by referencing to the X = 0, Y = 0 coordinates, which are located at the lower left corner. In relative mode, cursor movements are with respect to the previous cursor position.

The format of the data sent by the mouse is translated into a format that the CPU can understand.

All data transferred between the pointing device and the keyboard uses the following TTL level signals:

- 0 to 0.8 V dc = logic 1 = Mark = Off
- 2.0 to 5.0 V dc = logic 0 = Space = On

13.1 Pointing Device–to–Keyboard Quadrature Signals

For quadrature pointing devices, the clock edges of YA, YB, XA, and XB describe the motion. Upward motion is expressed when YA leads YB. Rightward motion is expressed when XA leads XB. Conversely, when nA lags nB, the opposite direction is expressed (n = Y or X). SWM, SWR, and SWL are active low, producing a button event (see Figure 13–1).

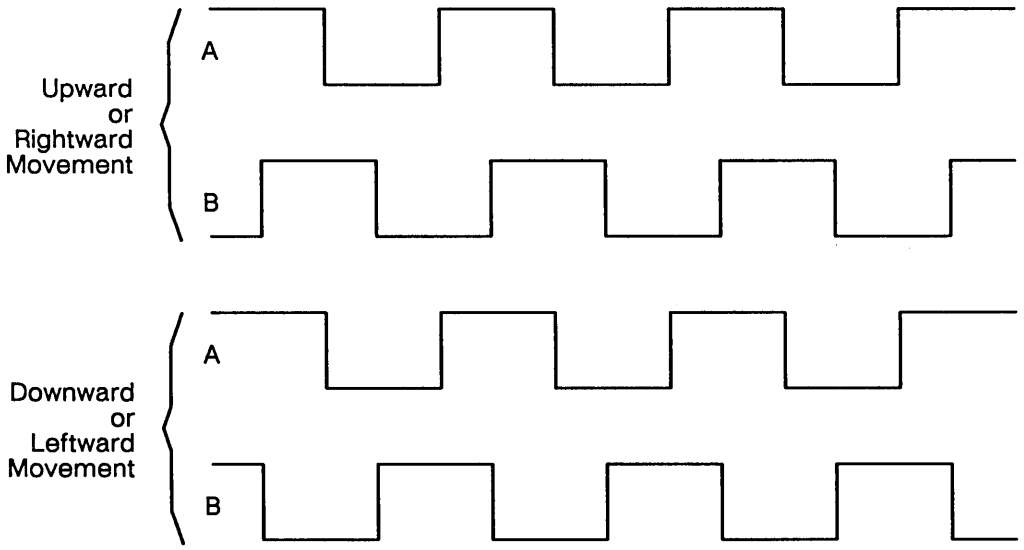


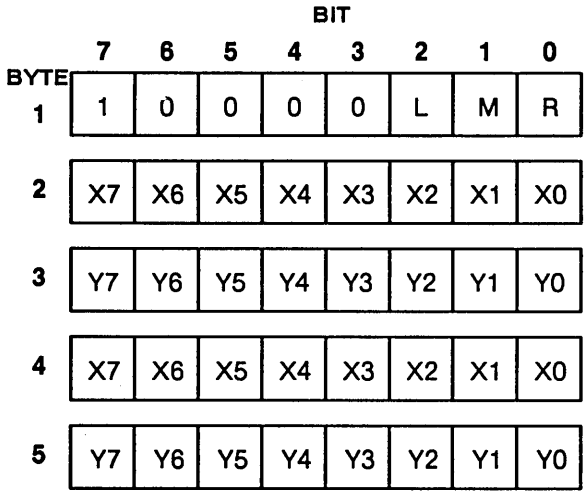
Figure 13–1. Quadrature Clock Signals

13.2 Pointing Device–to–Keyboard Serial Data Packets

A quadrature pointing device transmits data in relative mode only; a serial pointing device is capable of transmitting data in relative mode or absolute mode.

13.2.1 Relative Mode Format

The keyboard supports a 5–byte, packed–binary, serial–data format. In this format, data is transferred in the form of 8–bit bytes (8 bits without parity). One byte of key information and two successive data reports are sent. The second set of X and Y data (bytes 4 and 5) are possible overflow from the first report and the movement of the pointing device during transmission of the first report (see Figure 13–2 for packet bit assignments).

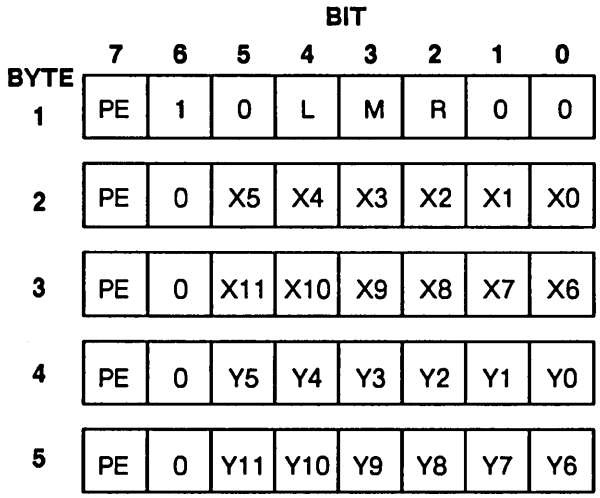


L, M, R = Left, Middle, Right Switch Data; 0 = switch depressed
X0 – X7 = X coordinate in signed Two's complement representation
Y0 – Y7 = Y coordinate in signed Two's complement representation

Figure 13–2. Relative Mode Data Packets

13.2.2 Absolute Mode Format

The keyboard supports the absolute Bit Pad One packed–binary, serial–data format. In this format, data is transferred in the form of 8–bit bytes (7 data bits plus parity). One byte of key information and two successive data reports are sent, one for X and one for Y. The X and Y are absolute coordinates of the pointing device position. Figure 13–3 shows the packet bit assignments.



L, M, R = Left, Middle, Right Switch Data; 1 = switch depressed
X0 to X11 = X coordinate in unsigned representation (0 to 4095)
Y0 to Y11 = Y coordinate in unsigned representation (0 to 4095)
PE = Even Parity

Figure 13–3. Absolute Mode Data Packets

13.3 Keyboard-to-CPU Data Packets

As stated in Chapter 12, the keyboard is capable of transmitting key scan codes to the host in one of two modes, Mode 0 (compatibility mode), and Mode 1 (keystate mode). In Mode 0, pointing device data is "escaped" by a special code, DF for relative and E8 for absolute data. In Mode 1, no such escape codes exist. Rather, there are distinct modes which are used for pointing device data, Mode 2 for relative and Mode 3 for absolute data. The formats for each of the data packets are described in Subsections 13.3.1 through 13.3.3.

13.3.1 Mode 0 - Cursor Control Data Packet Information

Relative cursor control coordinates, in the form of a packet message, are transmitted via the serial data line. This message contains an escape code (DF) as the first byte followed by three bytes of data. The second byte contains the three switches from the mouse and X and Y invalid indicators. SWM, SWR, and SWL are Zero if the switch is depressed. The X and Y bits are Zero when the data for the corresponding direction is valid. The third and fourth bytes contain the X and Y count values, respectively. The X and Y relative counts can range from +127 to -128. A positive count means that the pointing device is moving up or right, while a negative count means the pointing device is moving down or left. X and Y are signed Two's complement notation (see Figure 13-4 for packet bit assignments).

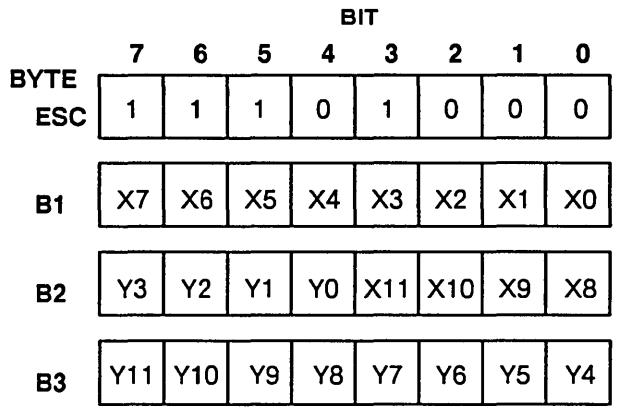
	BIT 7	6	5	4	3	2	1	0
BYTE ESC	1	1	0	1	1	1	1	1
B1	1	M	R	L	Y	Y	X	X
B2	X7	X6	X5	X4	X3	X2	X1	X0
B3	Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0

L, M, R = Left, Middle, Right Switch Data; 0 = switch depressed
X0 - X7 = X coordinate in signed Two's complement representation
Y0 - Y7 = Y coordinate in signed Two's complement representation

The bits are labeled such that the higher numbers are the more significant bits. A start, stop, and even parity bit must be added to the above data for a complete message. Bit 0 is sent first and bit 7 is sent last in the data stream.

Figure 13-4. Mode 0 Relative Cursor Movement

Absolute cursor coordinate information in the form of a packet message contains an escape code (E8) and three bytes of data that are the X and Y coordinate values. Figure 13-5 shows how the message is packed.



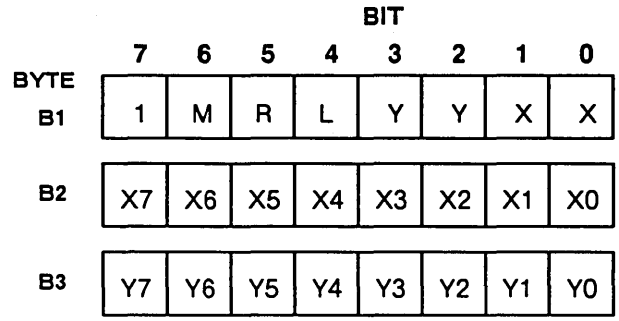
The bits are labelled such that the higher numbers are the more significant bits.

Figure 13–5. Mode 0 Absolute Cursor Movement

13.3.2 Mode 2 – Relative Cursor Control

In this mode, all transmissions are relative cursor coordinate information packets.

The first byte contains the three switches from the mouse and the X and Y invalid indicators. M, R, and L are a Zero if the switch is depressed. The X and Y bits are Zero when the data for the corresponding direction is valid. The second and third bytes contain the X and Y count values, respectively. The X and Y relative counts can range from +127 to −128. A positive count means the pointing device is moving up or right, while a negative count means the pointing device is moving down or left. X and Y are signed Two's complement notation. Figure 13–6 shows the packet bit assignments.



L, M, R = Left, Middle, Right Switch Data; 0 = switch depressed
X0 to X7 = Y coordinate in signed Two's complement representation
Y0 to Y7 = Y coordinate in signed Two's complement representation

The bits are labelled such that the higher numbers are the more significant bits. A start, stop, and even parity bit must be added to the above data for a complete message. Bit 0 is sent first and bit 7 is sent last in the data stream.

Figure 13–6. Mode 2 Relative Cursor Movement

13.3.3 Mode 3 – Absolute Cursor Control

In this mode, all transmissions are absolute cursor coordinate information packets transmitted as three bytes of data that are the X and Y coordinate values. Figure 13–7 shows how the message is packed.

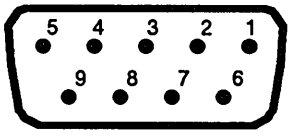
BYTE	BIT 7	6	5	4	3	2	1	0
B1	1	M	R	L	0	0	0	0
B2	X7	X6	X5	X4	X3	X2	X1	X0
B3	Y3	Y2	Y1	Y0	X11	X10	X9	X8
B4	Y11	Y10	Y9	Y8	Y7	Y6	Y5	Y4

The bits are labelled such that the higher numbers are the more significant bits.

Figure 13–7. Mode 3 Absolute Cursor Movement

13.4 Interface Connector

The mouse connector at the keyboard is a 9-pin, male, D-subminiature type (see Figure 13–8).



Pin	Signal – Quadrature	Serial
1	– +5 V	+5 V
2	– YB	TX
3	– YA	No connection*
4	– XB	No connection*
5	– XA	No connection*
6	– Logic Ground	Logic Ground
7	– SWM (middle switch)	No connection*
8	– SWR (right switch)	No connection*
9	– SWL (left switch)	No connection*
SHIELD	– Chassis Ground	Chassis Ground

Figure 13–8. Pointing Device Connector

Chapter 14

802.3 Network Controller–AT

14.1 Introduction

This chapter describes the 802.3 Network Controller–AT for the AT–compatible bus used with the *Domain System* workstation. The 802.3 Network Controller–AT enables a DS3000 or DS4000 to communicate over an IEEE/ETHERNET* 802.3 network.

The first 802.3 Network Controller–AT in a system uses interrupt line IRQ10 and DMA request line DRQ6; the second one uses interrupt line IRQ9 and DMA request line DRQ3.

The *Domain System* 802.3 Network Controller–AT has the following features:

- Full compliance with IEEE 802.3 standards
- Interoperable with Version 1.0 and Version 2.0 ETHERNET stations on the ETHERNET cable
- Controller must work with 802.3 transceivers and is qualified to work with multiport or fanout transceiver boxes
- Two cable taps supported, Vampire tap and BNC tap
- On–board, jumper–selectable transceiver for Thin ETHERNET with BNC connector and 15–pin "DIX" connector for use with external transceiver on rear panel
- 8–MHz MC80186 on–board processor
- 128 KB of on–board memory expandable to 512 KB
- Intel 82586 ETHERNET LAN coprocessor

* ETHERNET is a registered trademark of Xerox Corp.

14.2 Bus Interface

Refer to Chapter 2 of this book for AT-compatible bus interface information. The main CPU controls the 802.3 Network Controller-AT board's operation through the AT-compatible bus interface. The controller is a Slave device on the bus.

14.3 Packaging Characteristics

The 802.3 Network Controller-AT is a standard AT-compatible printed circuit board, approximately 33.35 cm x 10.67 cm (13.13 inches x 4.2 inches). The board can be plugged into one of the AT- or XT-compatible slots on the motherboard. Figure 14-1 shows the 802.3 Network Controller-AT PCB.

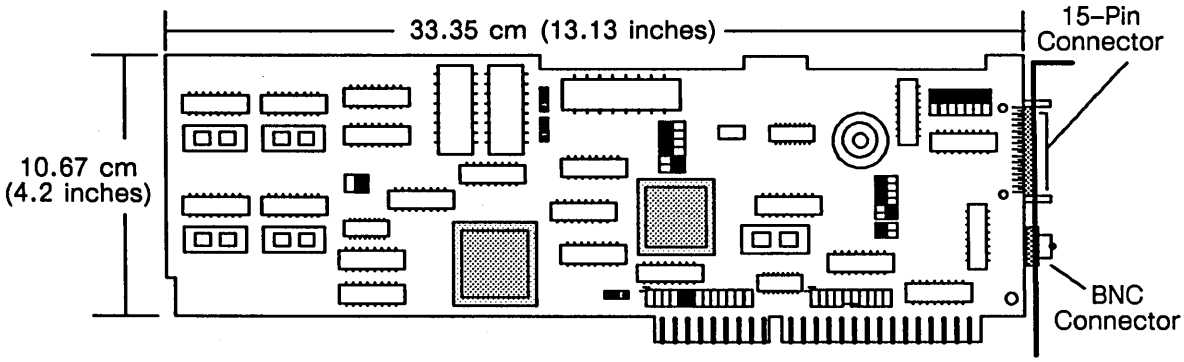
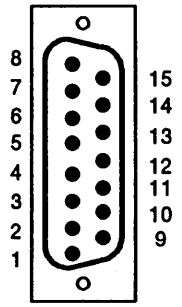


Figure 14-1. 802.3 Network Controller-AT PCB

14.4 External Connectors

The connector is an IEEE 802.3 and Version 2.0 compatible 15-pin, D-subminiature, female connector (Clinch type DA 51220-1). Figure 14-2 lists the external connector pin assignments.

Pin Number	Assignment
1	GND
2	Collision +
3	Transmit +
4	GND
5	Receive +
6	Power Return
7	Unused
8	GND
9	Collision -
10	Transmit -
11	GND
12	Receive -
13	Power
14	GND
15	Unused



External Connector

Pins 1, 4, 8, 11, and 14 are inner shield grounds. The outer shield should be terminated to the connector shell.

Figure 14-2. Transceiver Cable Connector Pin Assignemnts

14.5 Jumper Configuration

Figure 14–3 shows the jumper configuration for the 802.3 Network Controller–AT when it is plugged into an AT–compatible slot with the external tranceiver selected on the *Domain System* workstation.

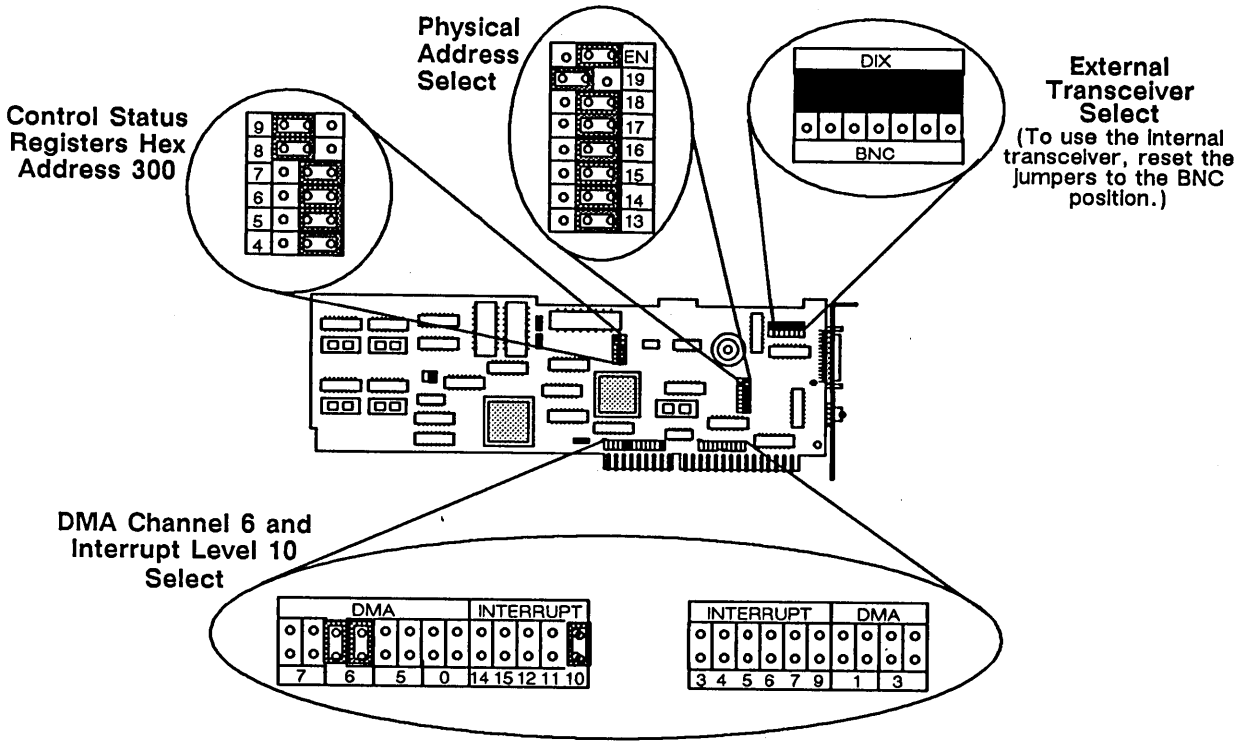


Figure 14–3. Standard 802.3 Network Controller–AT Jumper Configuration (AT–Compatible Slot)

Figure 14–4 shows the jumper configuration for the 802.3 Network Controller–AT when it is plugged into an XT–compatible slot with the external tranceiver selected on a *Domain System* workstation.

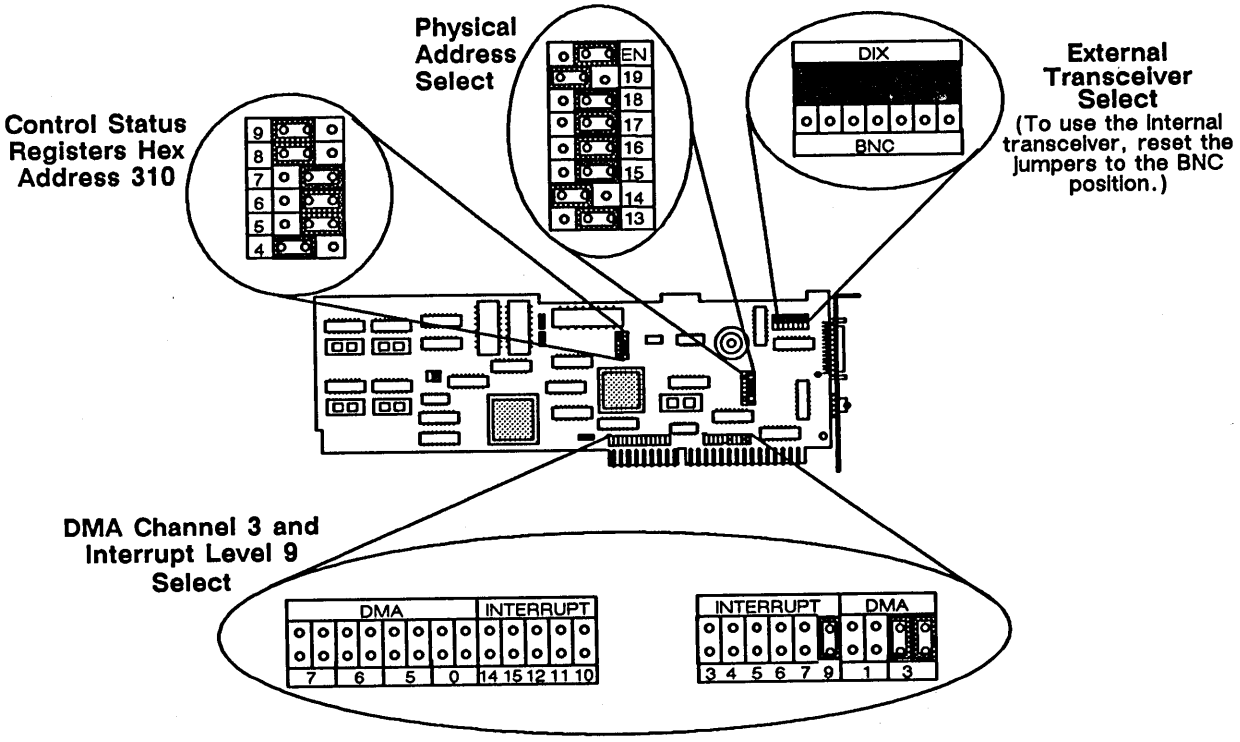


Figure 14–4. Alternate 802.3 Network Controller–AT Jumper Configuration (XT–Compatible Slot)

14.6 Voltage and Power Requirements

The following power is consumed by the 802.3 Network Controller–AT board:

- 1.7 amps on the +5 V
- 0.4 amp on the +12 V

14.7 Cooling Requirements

The heat dissipated by the 802.3 Network Controller–AT is removed by forced air cooling. The system fan generates a suitable air flow across the board for proper cooling.

Chapter 15

Serial/Parallel Controller

15.1 Introduction

This chapter describes the specifications for the optional Serial/Parallel Controller used with *Domain System* workstations. The specifications define the requirements for an AT/XT-bus compatible controller board that includes two RS-232 serial ports and one Centronics equivalent parallel port. The board plugs into one AT/XT slot of the *Domain System*.

Three interrrupt lines are provided: IRQ4, IRQ7 and IRQ9 (this interrupt is IRQ2 on the connector, but programmed as IRQ9). The data path is 8 bits wide and the address path is 16 bits wide.

The Serial/Parallel Controller has the following features:

- Two RS-232 serial ports
- One Centronics equivalent parallel port

15.2 Bus Interface

Refer to Chapter 2 of this manual for AT-compatible bus interface information. The main CPU controls the Serial/Parallel Controller board's operation through the AT-compatible bus interface (the board plugs into an AT/XT-compatible slot on the bus). The controller is a Slave device on the bus.

15.3 Packaging Characteristics

The Serial/Parallel Controller from IDEAssociates is a smaller XT-size printed circuit board, approximately 12.95 cm x 10.29 cm (5.1 inches x 4.05 inches). The board plugs into one of the AT/XT-type slots on the motherboard. Figure 15-1 shows the IDEAssociates Serial/Parallel Controller PCB.

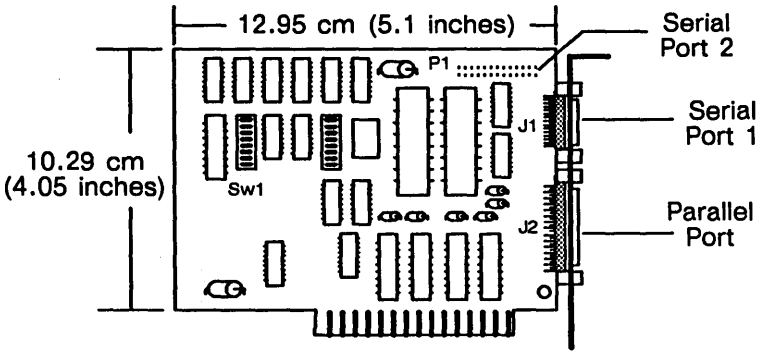


Figure 15-1. IDEAssociates Serial/Parallel Controller PCB

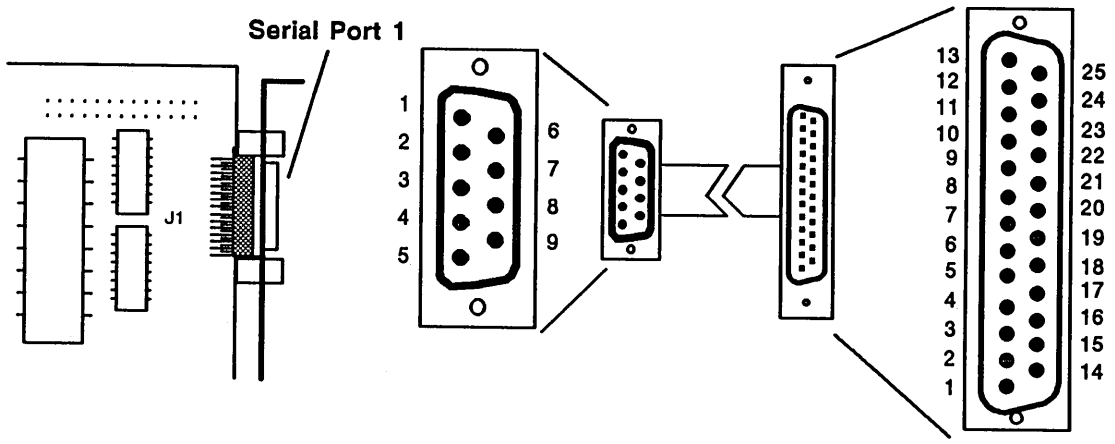
15.4 IDEAssociates I/O Connectors

This section lists the I/O connectors on the IDEAssociates board and the signals carried through them.

15.4.1 Serial Port 1

The external connector is a 9-pin, male, D-shell, metal-backed connector mounted on an L-shaped connector that is physically mounted to the controller board. The baud rates are programmable from 50 baud to 19,200 baud. The port generates interrupts on IRQ4.

Figure 15-2 shows the Serial Port 1 on the IDEAssociates serial/parallel board.



On-Board Connector Pin #	Signal Name	External Connector Pin #
6	Serial Data In	3
1	Serial Data Out	2
3	Data Set Ready (DSR)	6
7	Clear To Send (CTS)	5
4	Data Terminal Ready (DTR)	20
2	Request To Send (RTS)	4
8	Signal Ground	7
9	Carrier Detect	8
5	Ring Indicate	22
	Not Connected	All other pins

External Connector

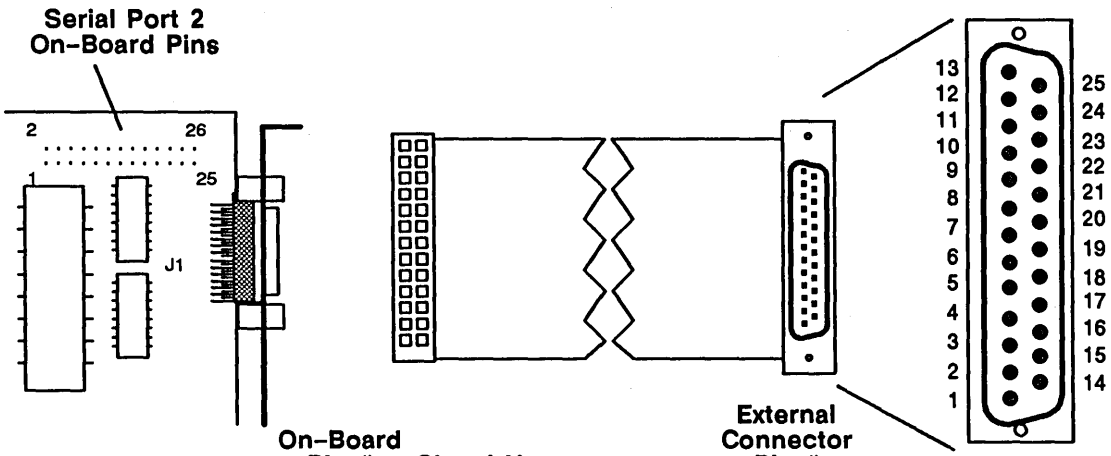
Figure 15–2. IDEAssociates Serial Port 1

15.4.2 Serial Port 2

Serial Port 2 is electrically and functionally equivalent to the specifications outlined for Serial Port 1 with the following exceptions:

- The connector is a 25-pin, female, D-shell, metal-backed connector mounted on an L-shaped bracket that is not connected to the controller board. A ribbon cable links the connector on one end to the set of pins on the controller board at the other end.
- The port generates interrupts on IRQ2 (logically connected to IRQ9).

Figure 15-3 shows the Serial Port 2 on the IDEAssociates serial/parallel board.



On-Board Pin #	Signal Name	External Connector Pin #
5	Serial Data In	3
3	Serial Data Out	2
11	Data Set Ready (DSR)	6
9	Clear To Send (CTS)	5
14	Data Terminal Ready (DTR)	20
7	Request To Send (RTS)	4
13	Signal Ground	7
15	Carrier Detect	8
18	Ring Indicate	22
*	Not Connected	*

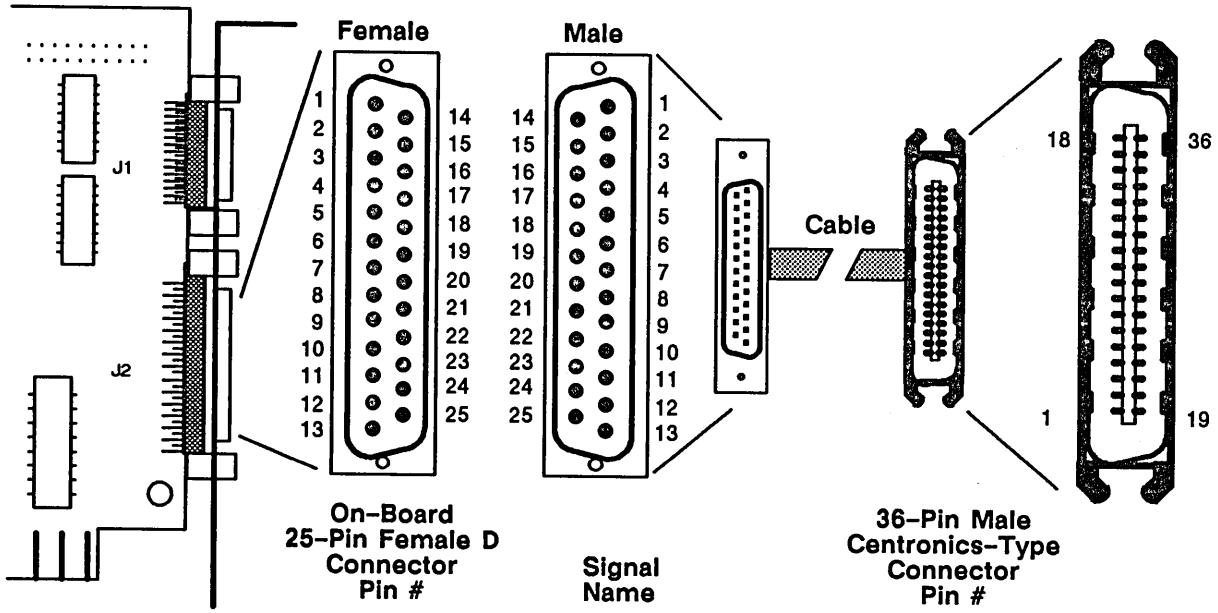
*** All other pins.**

Figure 15-3. IDEAssociates Serial Port 2

15.4.3 Parallel Port

The parallel port is functionally equivalent to the Centronics specification for printing devices. It is a 25-pin, female, metal, D-shell connector. All input and output signals conform to standard commercial TTL levels and temperature ranges. This port generates an interrupt on IRQ7 when an acknowledge pulse is received.

Figure 15–4 shows the parallel port on the IDEAssociates serial/parallel board.



On-Board 25-Pin Female D Connector Pin #	Signal Name	36-Pin Male Centronics-Type Connector Pin #
1	Strobe	1
2	Data Bit 0	2
3	Data Bit 1	3
4	Data Bit 2	4
5	Data Bit 3	5
6	Data Bit 4	6
7	Data Bit 5	7
8	Data Bit 6	8
9	Data Bit 7	9
10	Acknowledge	10
11	Busy	11
12	Paper Empty	12
13	Select	13
14	Auto Feed	Not Connected
15	Error	32
16	Initialize Printer	31
17	Select Input	Not Connected
18–25	Ground	19–26
	Not Connected	14 – 18, 27 – 30,
	Not Connected	33 – 36

Figure 15–4. IDEAssociates Parallel Port

15.5 Switchpack Settings

Figure 15–5 shows the switchpack settings for the IDEAssociates serial/parallel board.

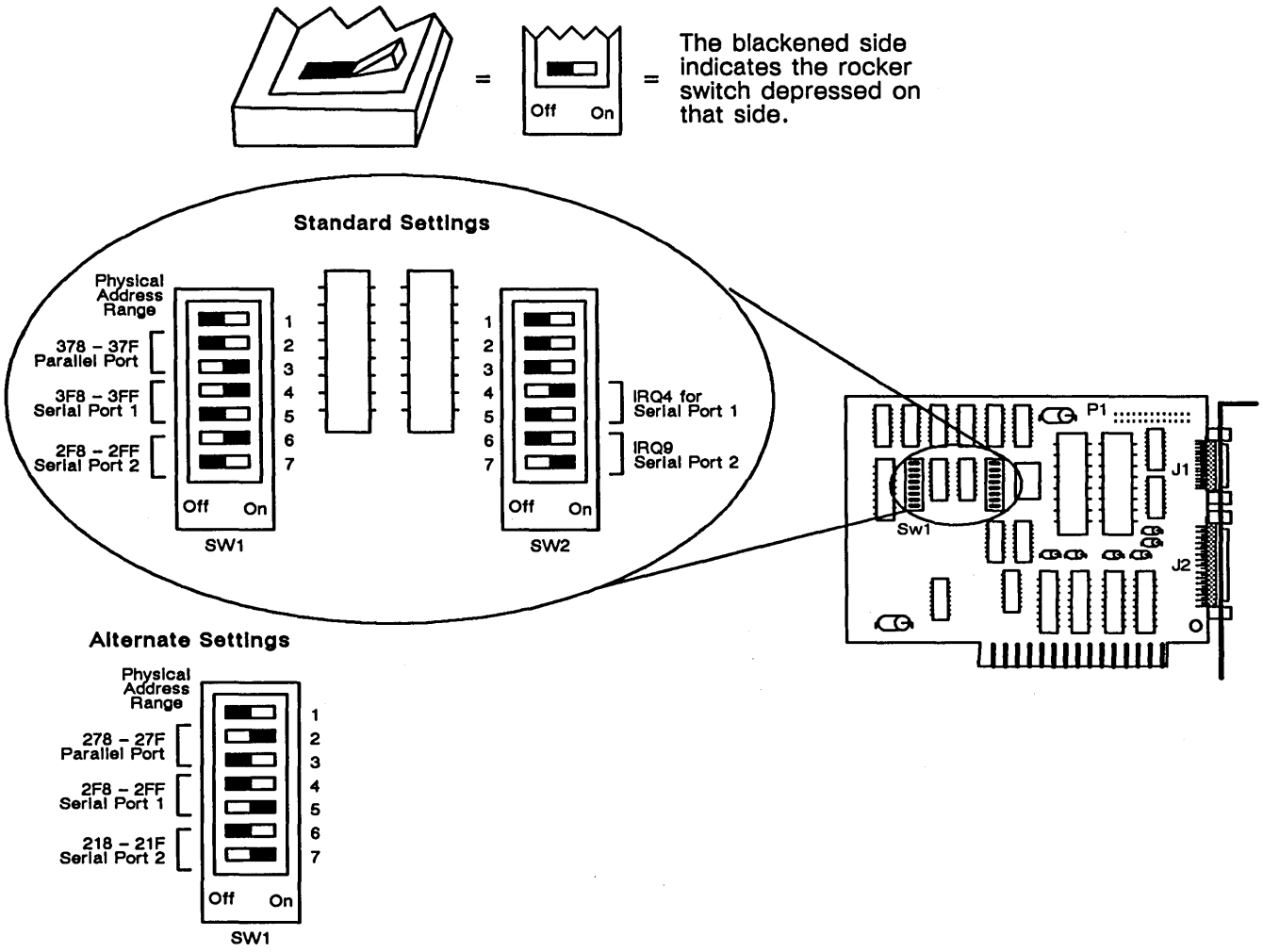


Figure 15–5. IDEAssociates Switchpack Settings

15.6 Voltage and Power Requirements

The following voltage is provided (via the motherboard) to the Serial/Parallel controller board:

- +5.0 V at 0.7 amp
- +12.0 V at 0.05 amp
- -12.0 V at 0.05 amp

15.7 Cooling Requirements

The heat dissipated by the Serial/Parallel Controller is removed by forced air cooling. The system fan generates suitable air flow across the board for proper cooling.

Chapter 16

PC Coprocessor

16.1 Introduction

This chapter describes the specifications for the PC Coprocessor used with the *Domain System* workstations. The specifications define the requirements for an AT-bus compatible controller board that is used to simulate the PC user environment and perform related functions on a Series 3000 or Series 4000 node. The board plugs into one AT-size slot of the *Domain System*.

The default interrupt line is IRQ11. The alternate interrupt line is IRQ15.

The default 16-bit DMA request line is DRQ5.

The PC Coprocessor features a socket for the optional MC80287 floating-point coprocessor.

16.2 Bus Interface

Refer to Chapter 2 of this manual for AT-compatible bus interface information. The main CPU controls the PC Coprocessor board's operation through the AT-compatible bus interface (the board plugs into an AT-compatible slot on the bus). The controller acts as a Slave device on the bus. However, when directing the actions of another PC-type adapter board (8- or 16-bit), the PC Coprocessor acts as a Master on the bus.

16.3 Packaging Characteristics

The PC Coprocessor is an AT-size printed circuit board, approximately 33.66 cm x 11.43 cm (13.25 inches x 4.5 inches). The board plugs into one of the AT-size slots on the motherboard. Figure 16-1 shows the PC Coprocessor PCB.

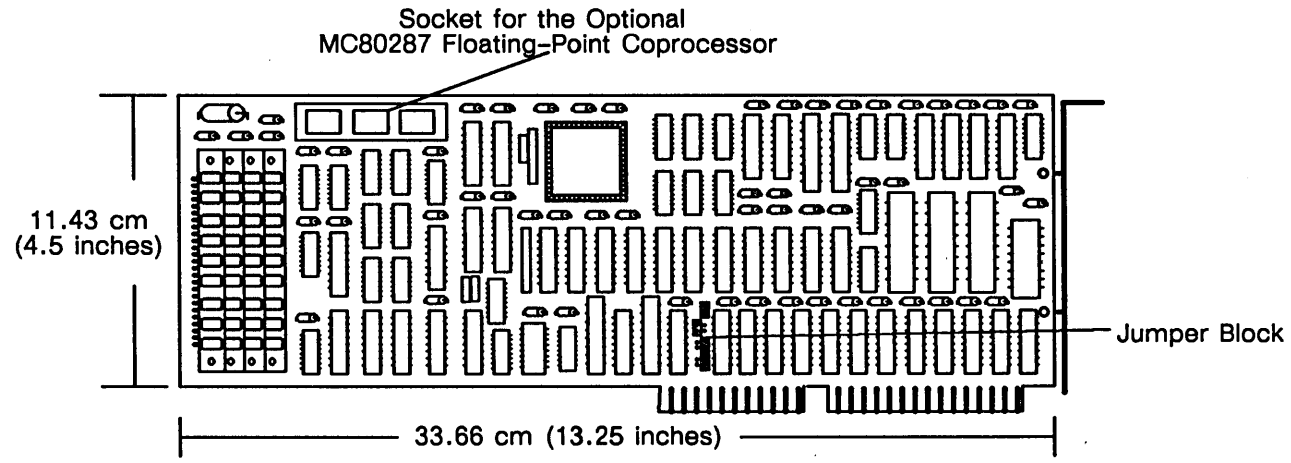


Figure 16-1. PC Coprocessor PCB

16.4 Jumper Configuration

Figure 16-2 shows the standard jumper configurations for the PC Coprocessor PCB.

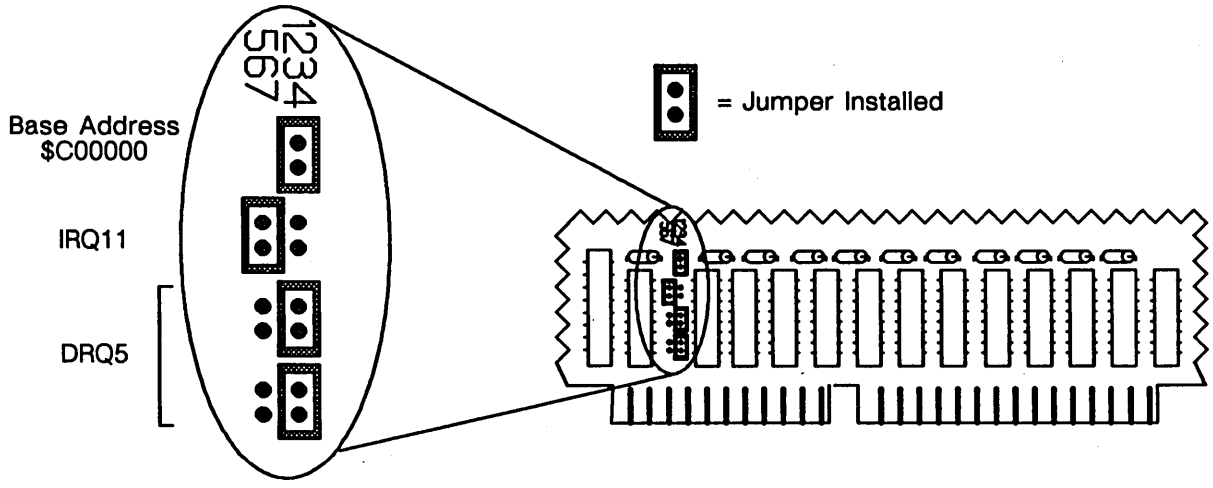


Figure 16-2. PC Coprocessor Standard Jumper Configuration

Figure 16–3 shows the alternate jumper configurations for the PC Coprocessor PCB.

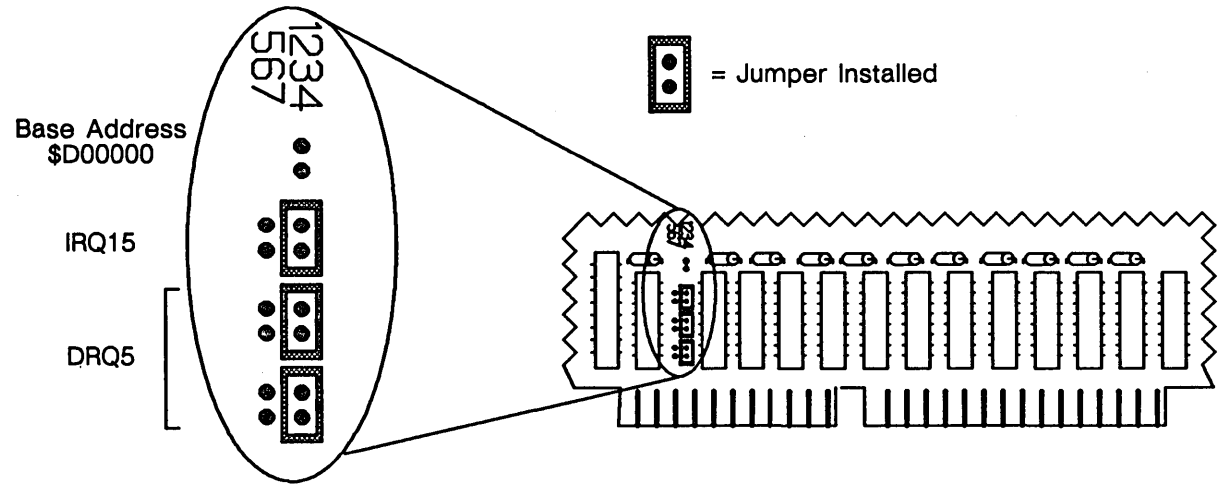


Figure 16–3. PC Coprocessor Alternate Jumper Configuration

16.5 Voltage and Power Requirements

The following voltage is provided (via the motherboard) to the PC Coprocessor board:

+5.0 V at 2.8 amps

16.6 Cooling Requirements

The heat dissipated by the PC Coprocessor PCB is removed by forced air cooling. For proper cooling, the system fan generates a suitable air flow across the board.

16.7 Environmental Specifications

The controller must operate error free with no derating of any specified operating or reliability parameter in the following environments:

- Temperature: 50° F to 100° F (10° C to 38° C)
- Altitude: 0 to 10000 feet (0 to 2.1 km)
- Humidity: 0% to 95% maximum
- Shock: 2.5 G peak (1/2 sine wave, 11–msec duration on any axis)
- Vibration: 0 to 63 Hz, 0.005 inches peak–to–peak, 63 to 500 Hz, 1.0 G peak maximum

Appendix A

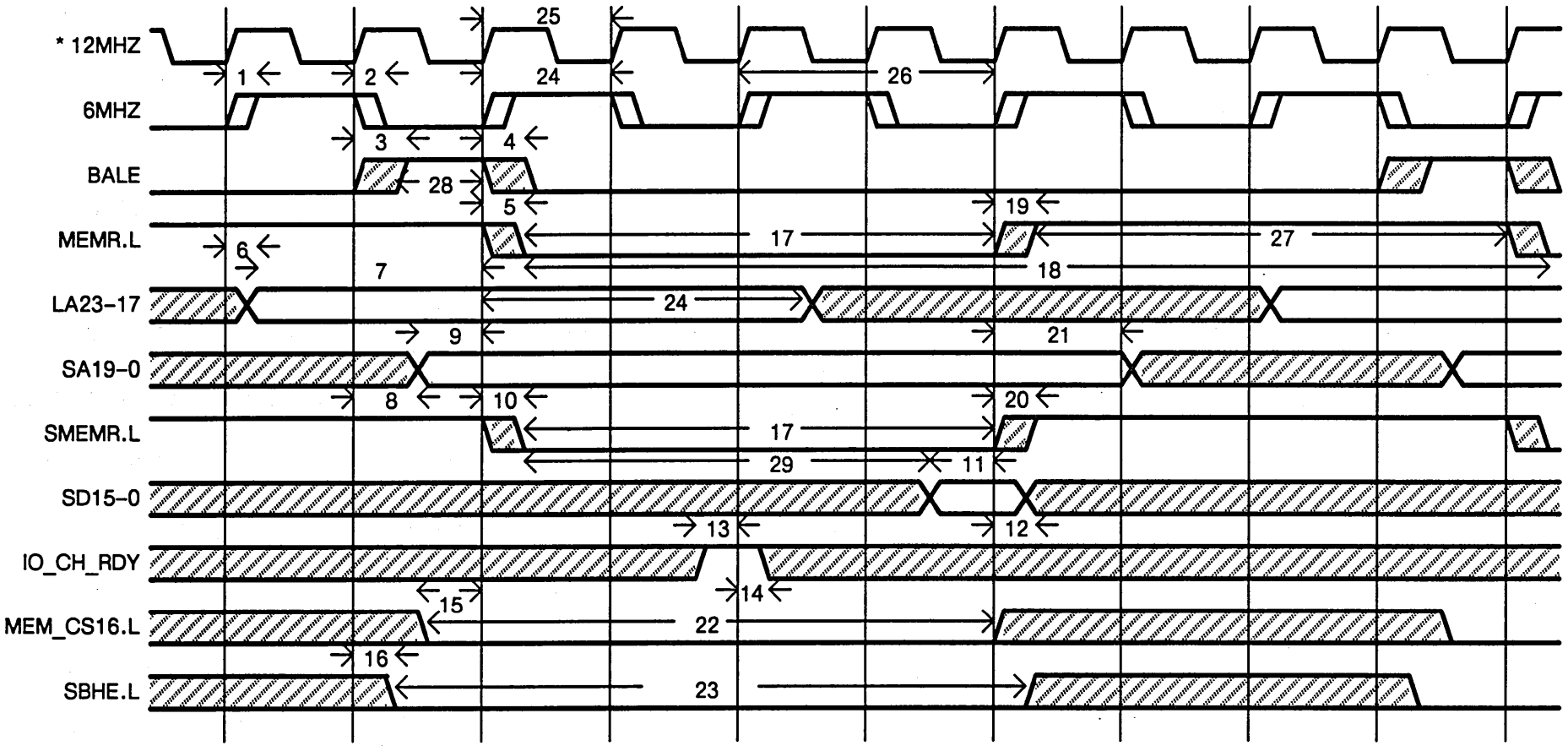
Series 3000 AT-Compatible Bus Timing Diagrams

This appendix contains timing diagrams for the 6-MHz AT-compatible bus processes in the Series 3000. Table A-1 contains reference information for the cycle times shown in the timing diagrams contained in this chapter. Find the reference number in a diagram and refer to the table for the correct cycle times.

Table A-1. Series 3000 AT-Compatible Bus Cycle Times

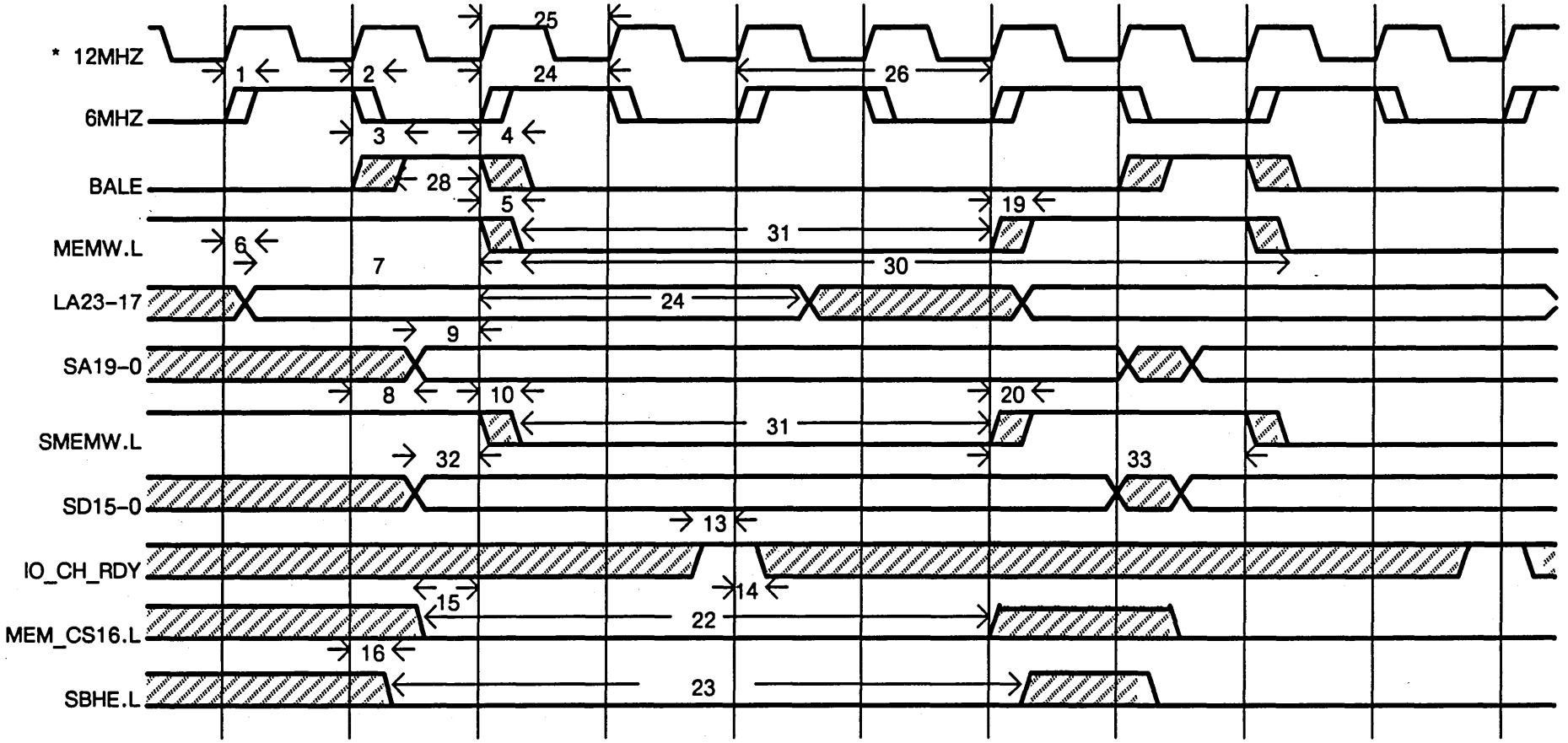
Number	Characteristic	Time (Nanoseconds) Minimum	Maximum
1	CLOCK High to BUS CLOCK High	0	15
2	CLOCK High to BUS CLOCK Low	0	15
3	CLOCK High to BALE High	0	30
4	CLOCK High to BALE Low	0	30
5	CLOCK High to MEMR.L Low	0	22
6	CLOCK High to LA23 - LA17 Valid	0	10
7	LA23 - LA17 Valid to MEMR.L Asserted	160	—
8	CLOCK High to SA19 - SA0 Valid	0	35
9	SA19 - SA0 Valid to MEMR.L Asserted	48	—
10	CLOCK High to SMEMR.L Asserted	0	22
11	SD15 - SD0 Valid to CLOCK High	30	—
12	CLOCK High to SD15 - SD0 Invalid	10	—
13	IO_CH_RDY Asserted to CLOCK High	20	—
14	CLOCK High to IO_CH_RDY Negated	10	—
15	MEM_CS16.L Asserted to CLOCK High	37	—
16	CLOCK High to SBHE.L Asserted	0	22
17	MEMR.L, SMEMR.L Width Asserted	330	—
18	Memory Read Cycle Time	666	—
19	CLOCK High MEMR.L Negated	0	22
20	CLOCK High SMEMR.L Negated	0	22
21	CLOCK High SA19 - SA0 Invalid	83	—
22	MEM_CS16.L Width Asserted	370	—
23	SBHE.L Width Asserted	400	—
24	BUS CLOCK Width High	75	90
25	12 MHz CLOCK Cycle Time	—	83
26	BUS CLOCK Cycle Time	—	166
27	MEMR.L Width High	330	—
28	BALE Width Asserted High	75	90
29	SD15 - SD0 Valid from MEMR.L Asserted	310	—
30	Memory Write Cycle Time	500	—
31	MEMW.L, SMEMW.L Width Asserted	330	—
32	SD15 - SD0 Valid to MEMW.L, SMEMW.L	20	—
33	MEMW.L, SMEMW.L Width Negated	166	—
34	SA19 - SA0 Valid to IOW.L Asserted	130	—
35	IO_CS16.L Width Asserted	200	—
36	IO_CS16.L to CLOCK High	37	—
37	IOR.L, IOW.L Width Asserted	250	—
38	SD15 - SD0 Valid from IOR.L, IOW.L High	60	—
39	SA19 - SA0 Valid from IOR.L, IOW.L High	60	—
40	SD15 - SD0 Valid to CLOCK High	30	—
41	CLOCK High to SD15 - SD0 Invalid	10	—
42	BALE.L to SMEMW.L Asserted	45	—
43	SMEMW.L Width Asserted	750	—
44	SA19 - SA0 Valid to SMEMW.L Asserted	130	—
45	MEM_CS16.L Negated to CLOCK High	37	—
46	SD Valid to SMEMW.L Asserted	100	—
47	SD Valid to IOW.L Asserted	100	—
48	IOR.L, IOW.L Width Asserted	750	—
49	IO_CS16.L Negated to CLOCK High	37	—
50	CLOCK High to IOR.L, IOW.L	0	22
51	CLOCK High to IOR.L, IOW.L Negated	0	22
52	CLOCK High to AEN Asserted	0	60
53	CLOCK High to AEN Negated	0	60
54	MEMR.L Width Asserted	333	—
55	BALE Width Asserted	830	—
56	SA7 - SA0 Valid to MEMR.L Asserted	166	—
57	CLOCK High to REFRESH.L Asserted	0	20
58	CLK Low to DACK High	—	170
59	CLK Low to AEN High	—	200
60	Address Float to Active from CLK High	—	170
61	READ or WRITE Active from CLK High	—	150
62	CLK High to READ or WRITE High	—	190
63	CLK High to WRITE High	—	130
64	CLK High to READ High	—	190
65	CLK High to TC High	—	170
66	CLK High to TC Low	—	170
67	DRQ to CLK Low Setup Time	0	—
68	CLK Low to DACK Low	—	170
69	CLK High to AEN Low	—	130
70	WRITE High to Address Hold Time	—	283
71	CLK High to READ or WRITE Float	—	120
72	MASTER.L Negated from DRQ Negated	—	250
73	SA19-0, LA23-17 Tristate Master Negated	—	50
74	DACK Asserted to MASTER.L Asserted	50	—
75	Bus Driven from MASTER Asserted	166	—
76	MEMCMD, IOCMD Asserted from Master.L	333	—
77	Master Width Asserted	—	12 µs
78	MEMR.L, SMEMR.L, 0WS Width Asserted	160	—
79	0WS to CLK High	50	—
80	MEMR/W, SMEMR/W, 0WS	415	—
81	MEMR.L to valid SD15-0	—	250
82	MEMR.L to SD15-0 invalid	—	80
83	IOR.L to SD15-0 valid	—	200
84	IOR.L to SD15-0 invalid	—	0

VCC = 4.75 V dc to 5.25 V dc TA = 0°to 70° C



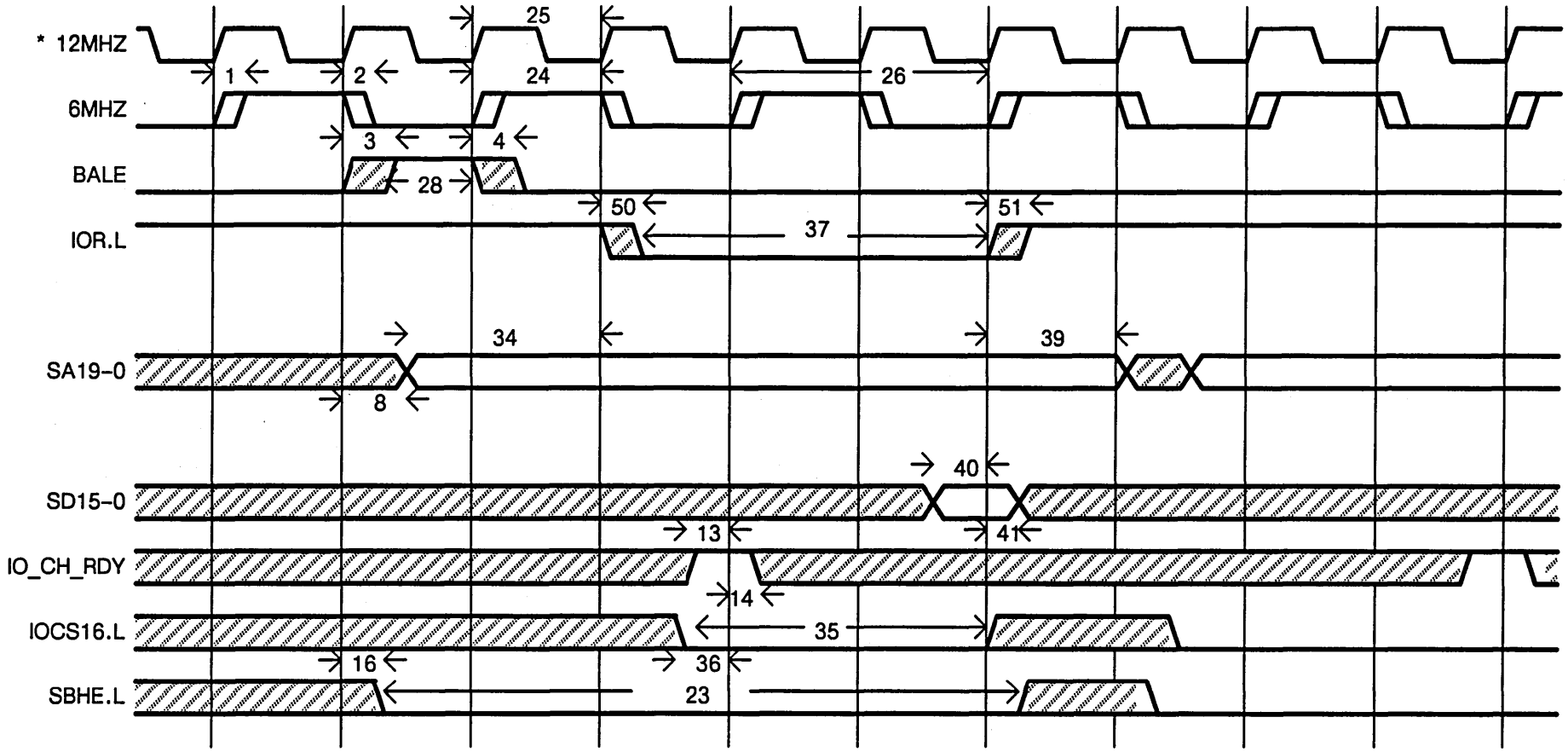
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-1. Bus 16-Bit Memory Read Cycle



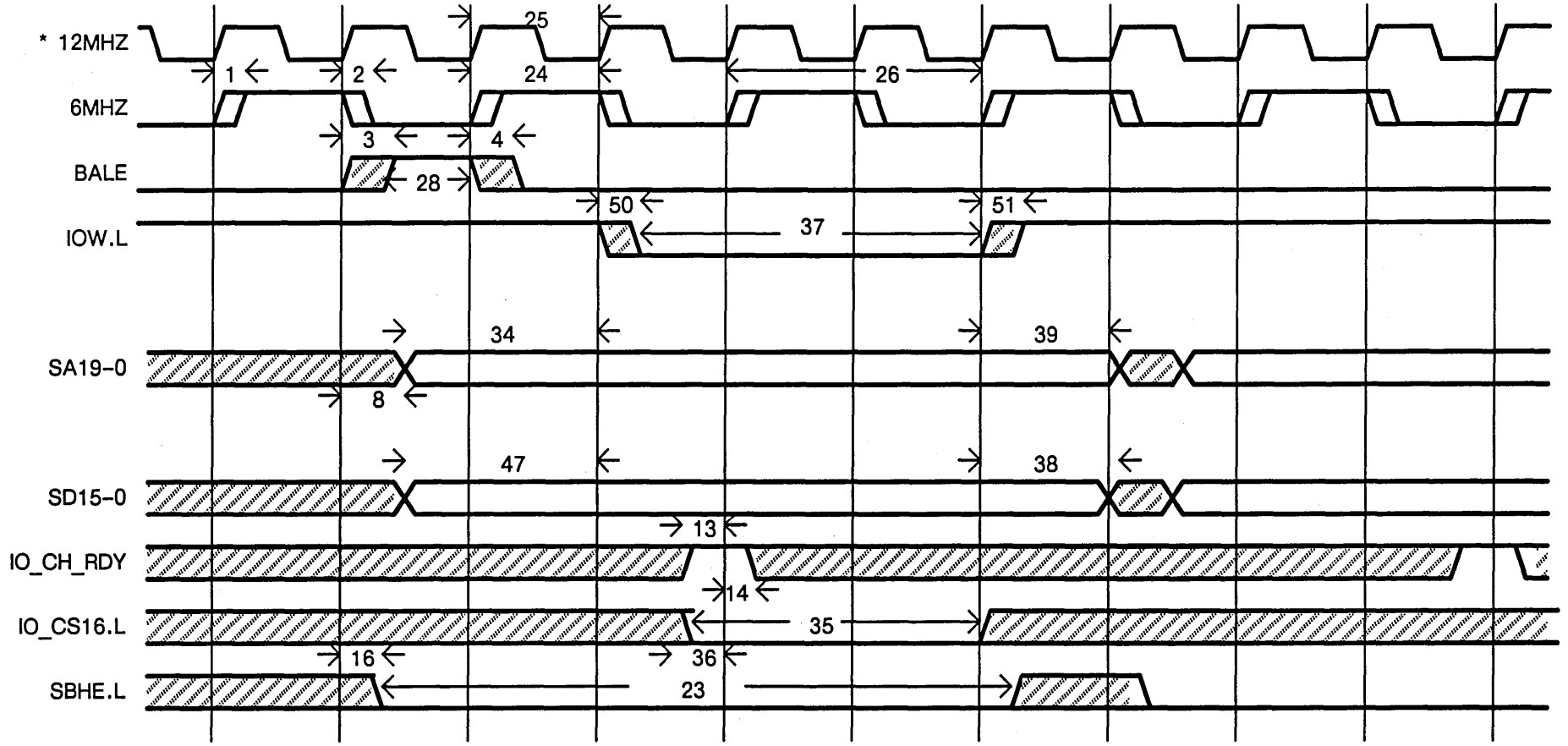
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-2. Bus 16-Bit Memory Write Cycle



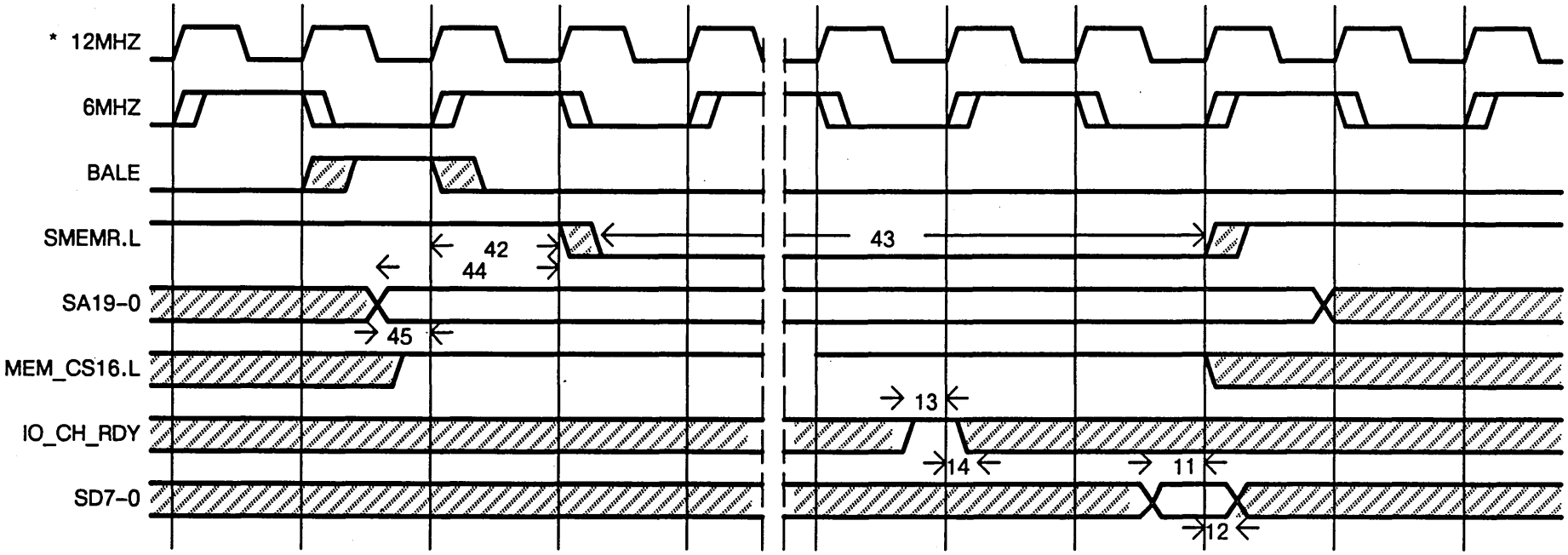
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-3. Bus 16-Bit I/O Read Cycle



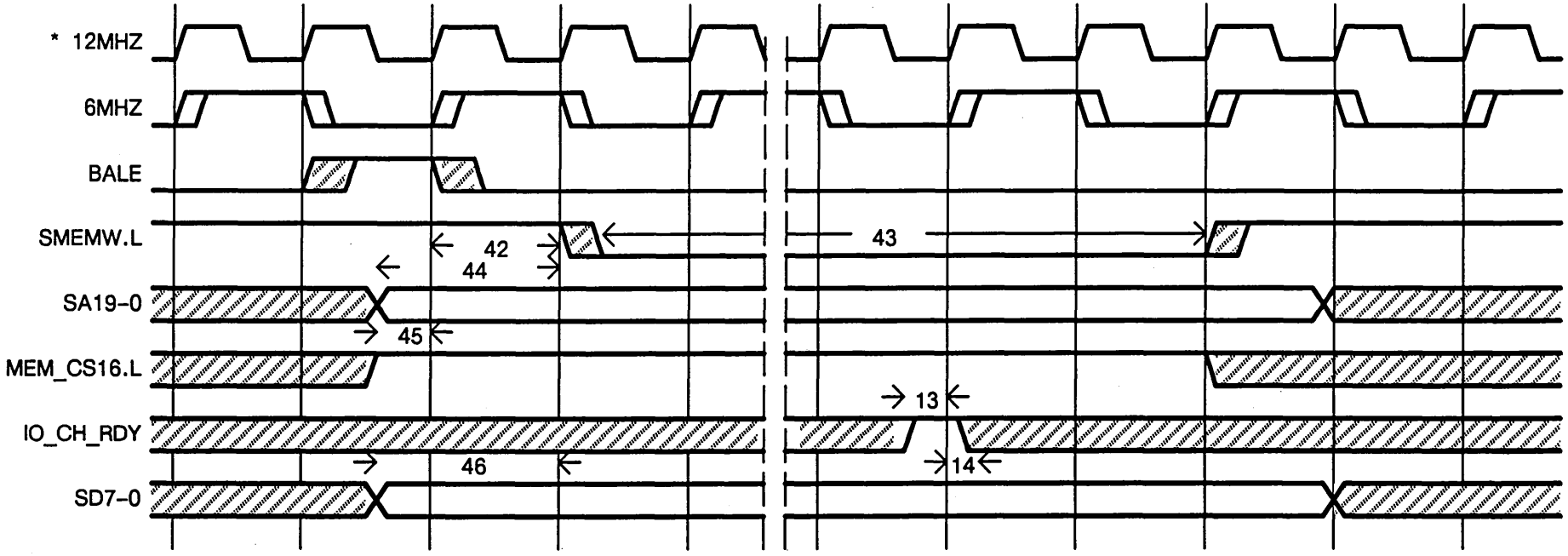
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A–4. Bus 16-Bit I/O Write Cycle



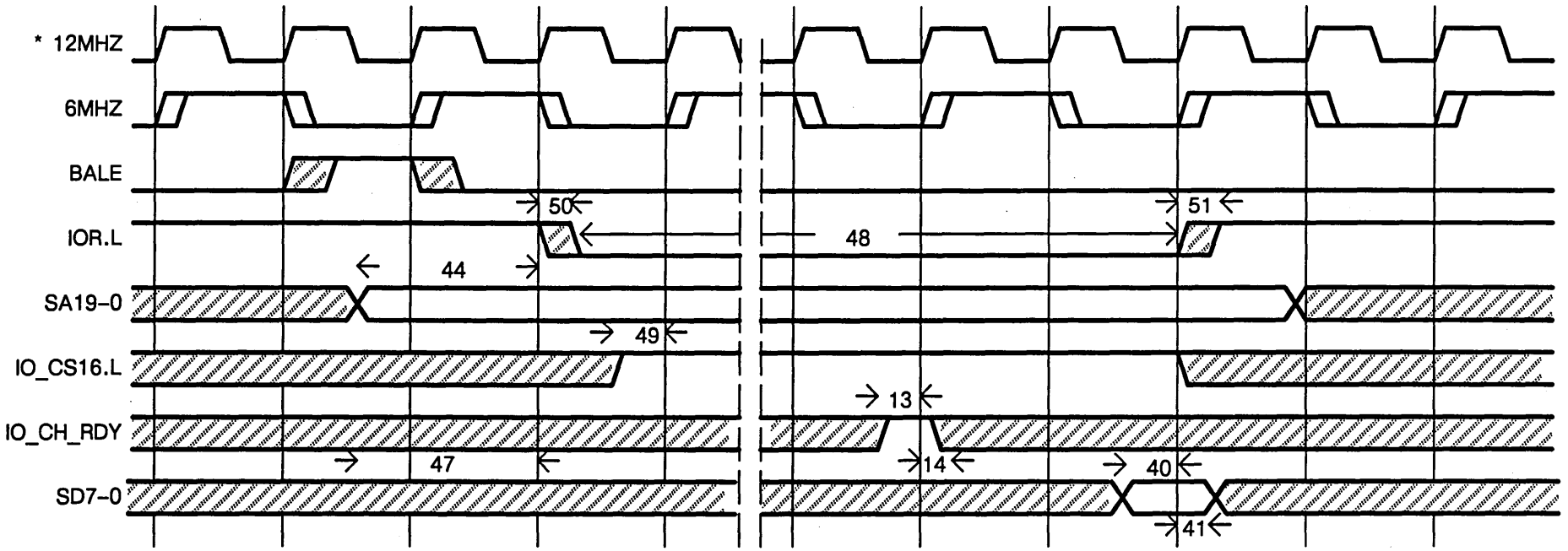
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-5. Bus 8-Bit Memory Read Cycle



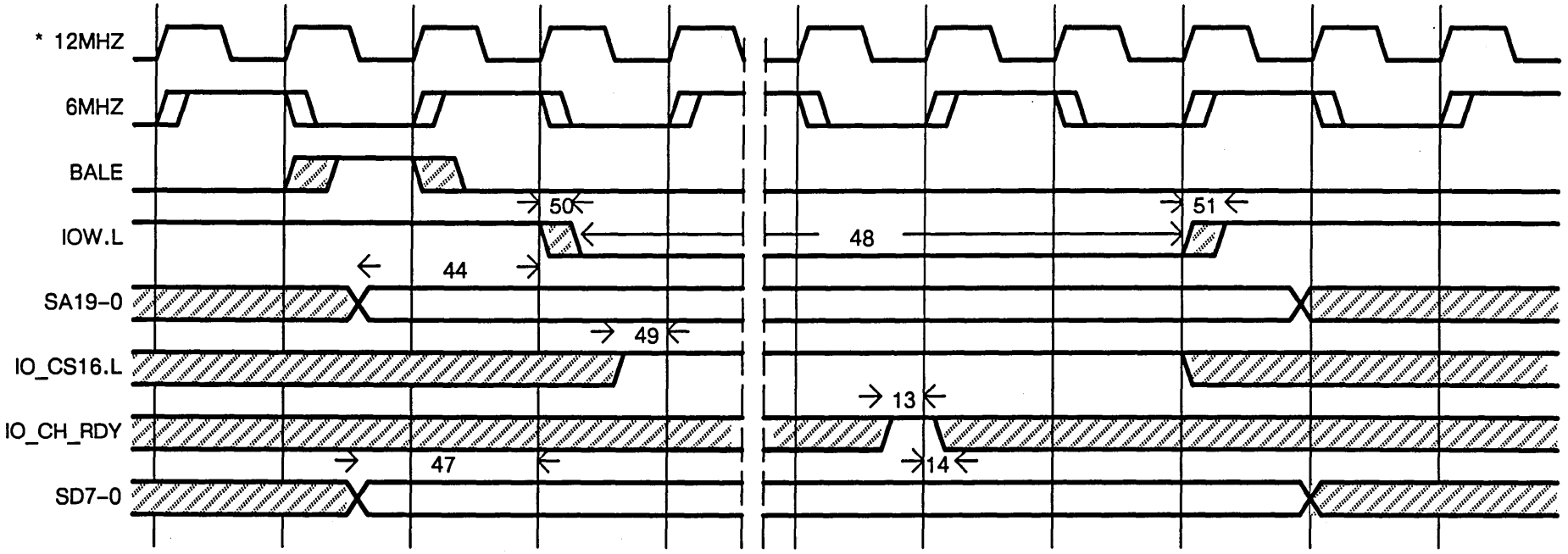
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-6. Bus 8-Bit Memory Write Cycle



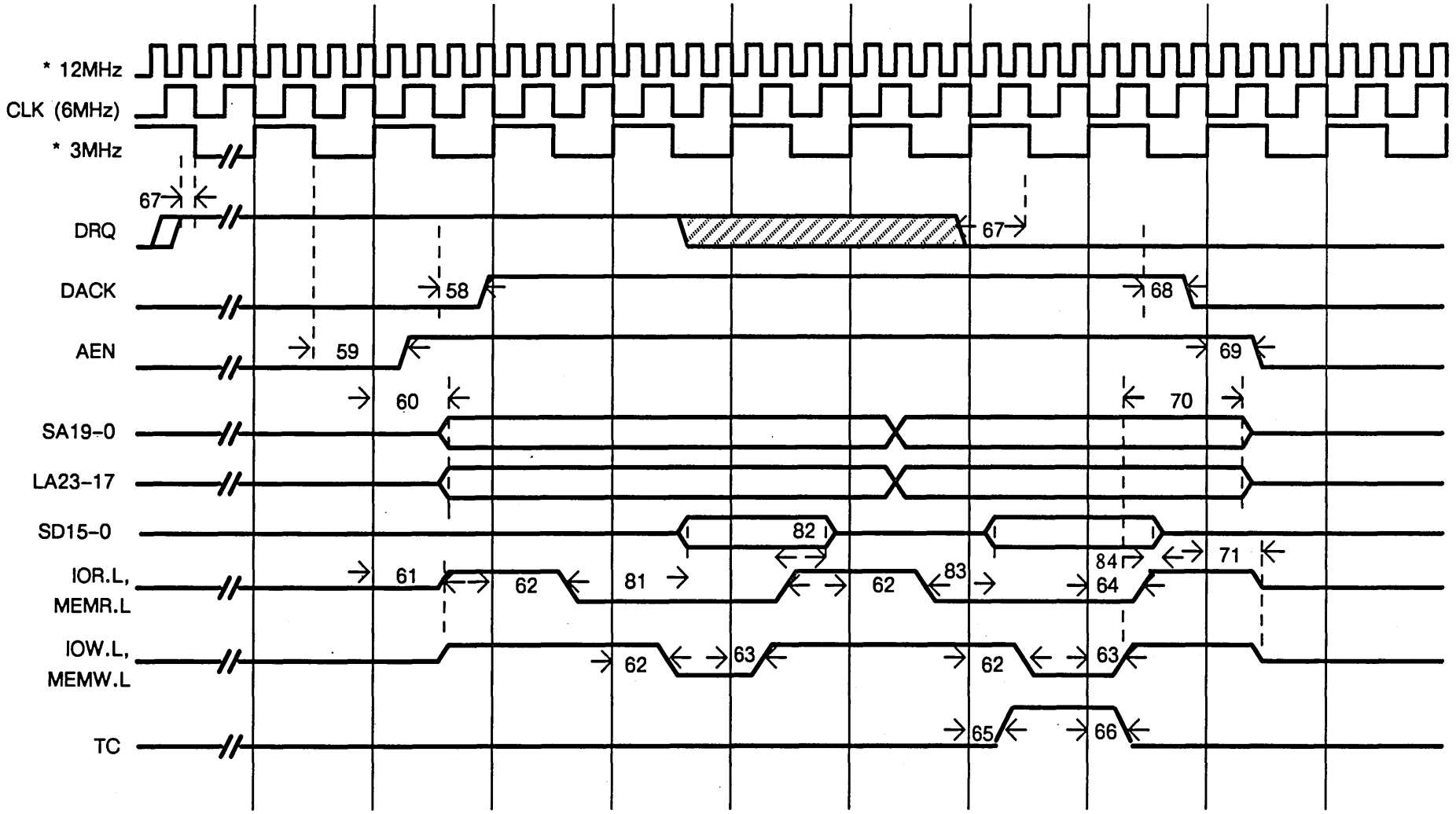
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-7. Bus 8-Bit I/O Read Cycle



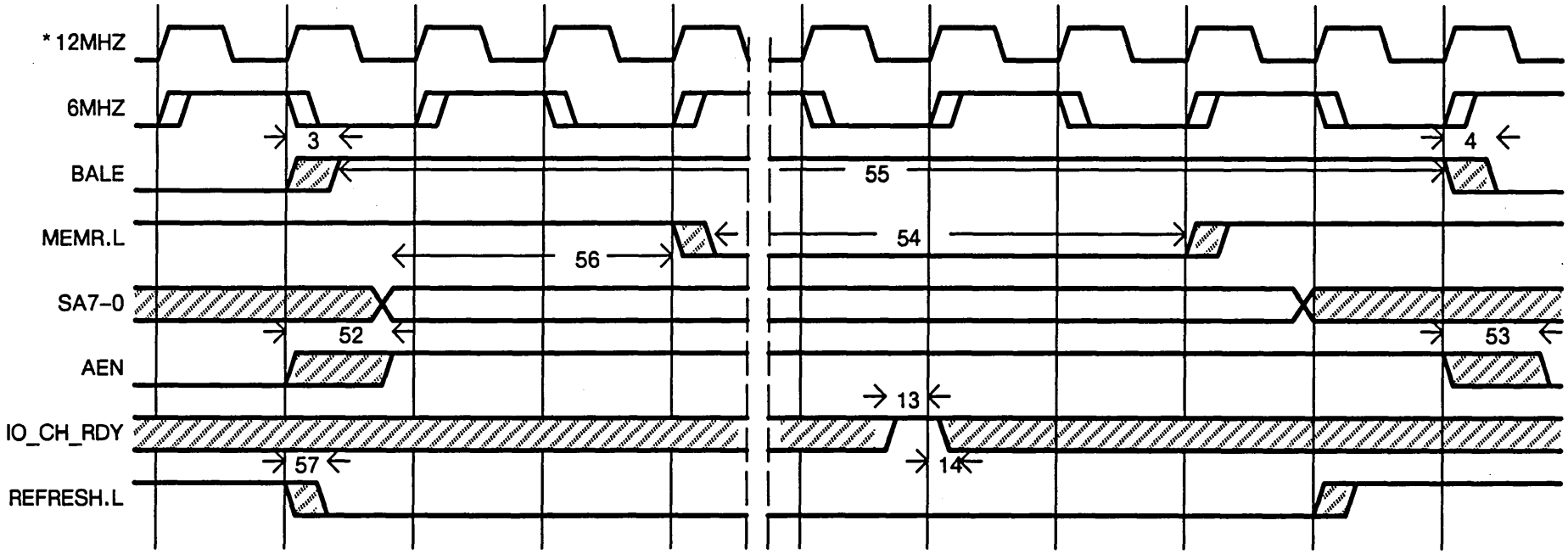
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-8. Bus 8-Bit I/O Write Cycle



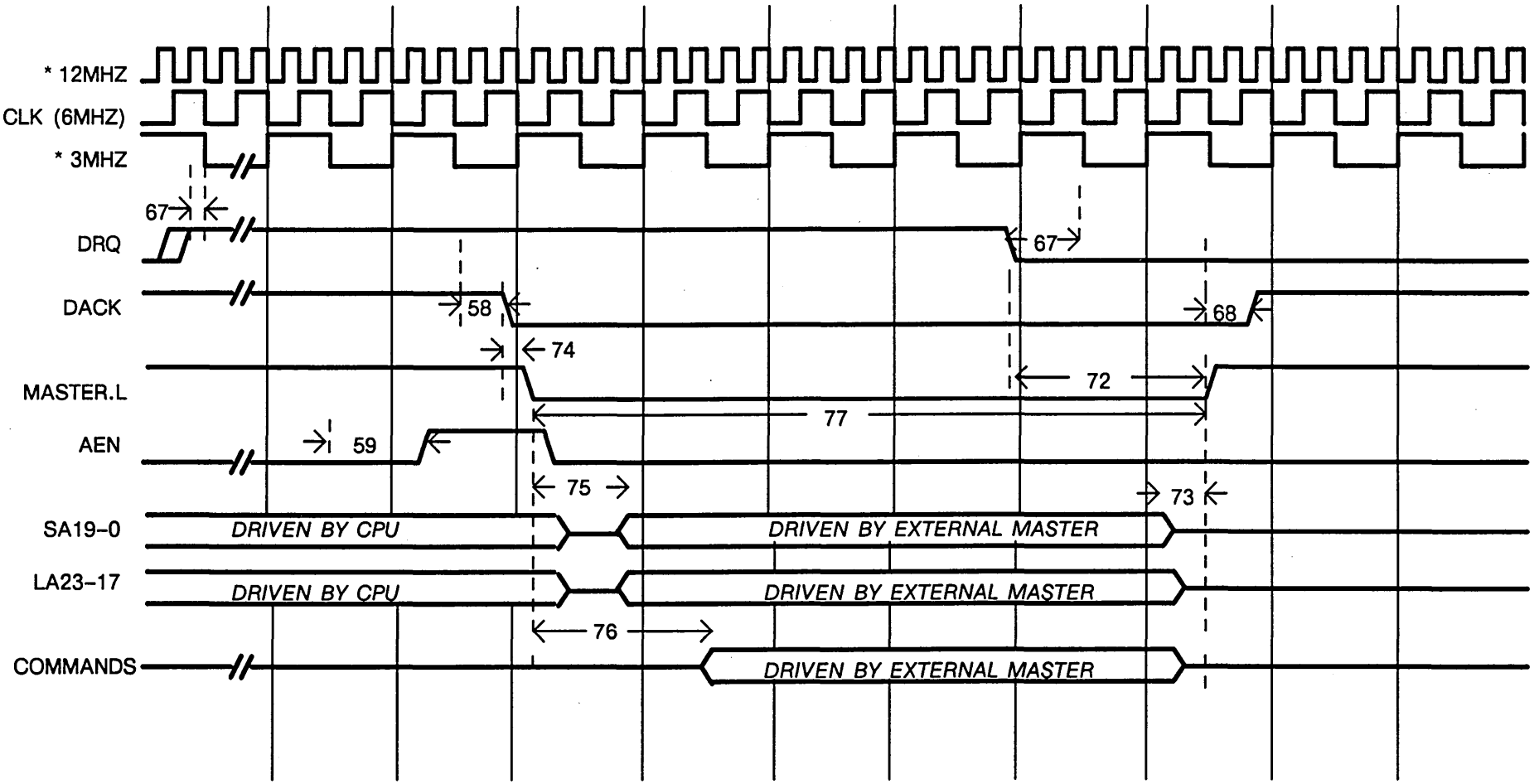
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-9 Bus DMA Cycles



* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-10. Bus Refresh Cycle



* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure A-11. External Mastership

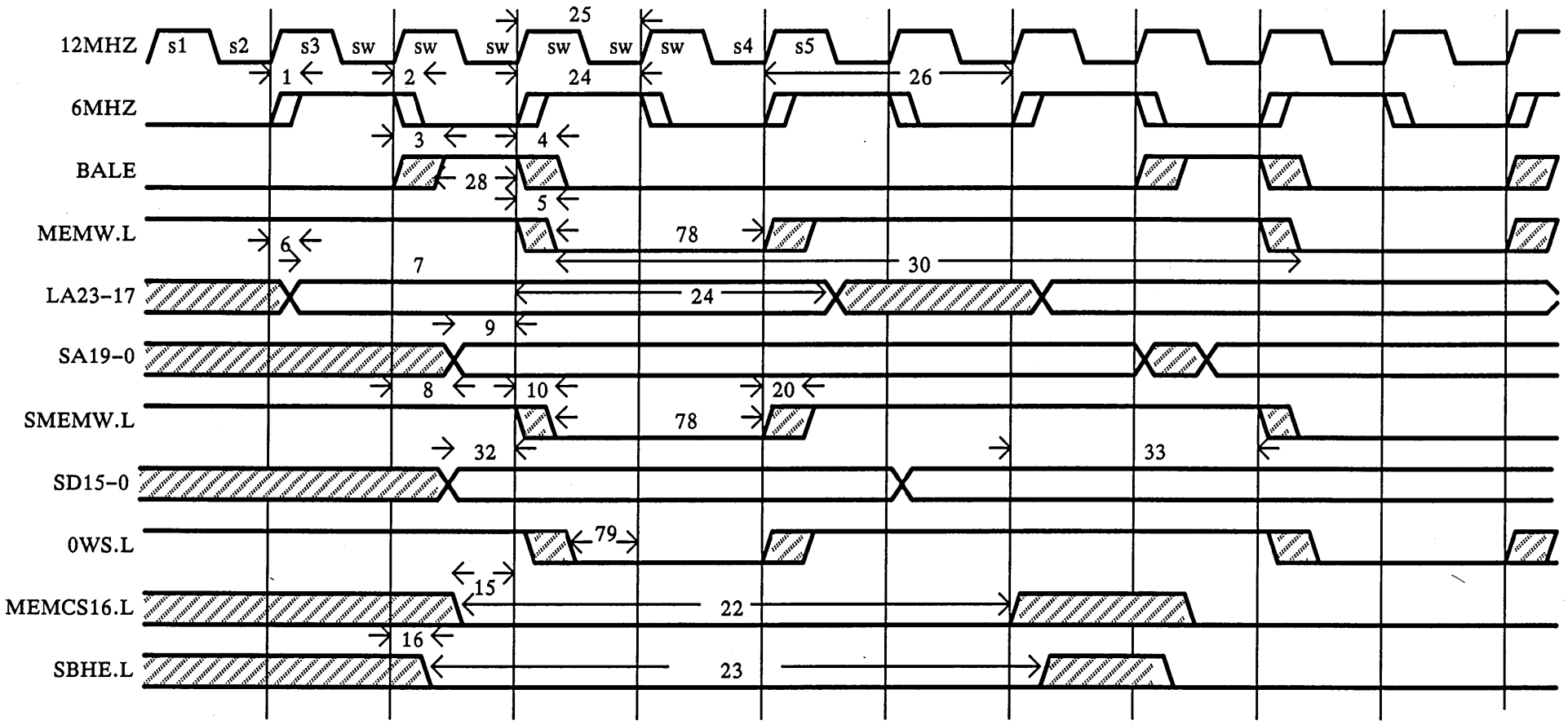


Figure A–12. Bus 16–Bit Memory Write Cycle (Zero Wait State)

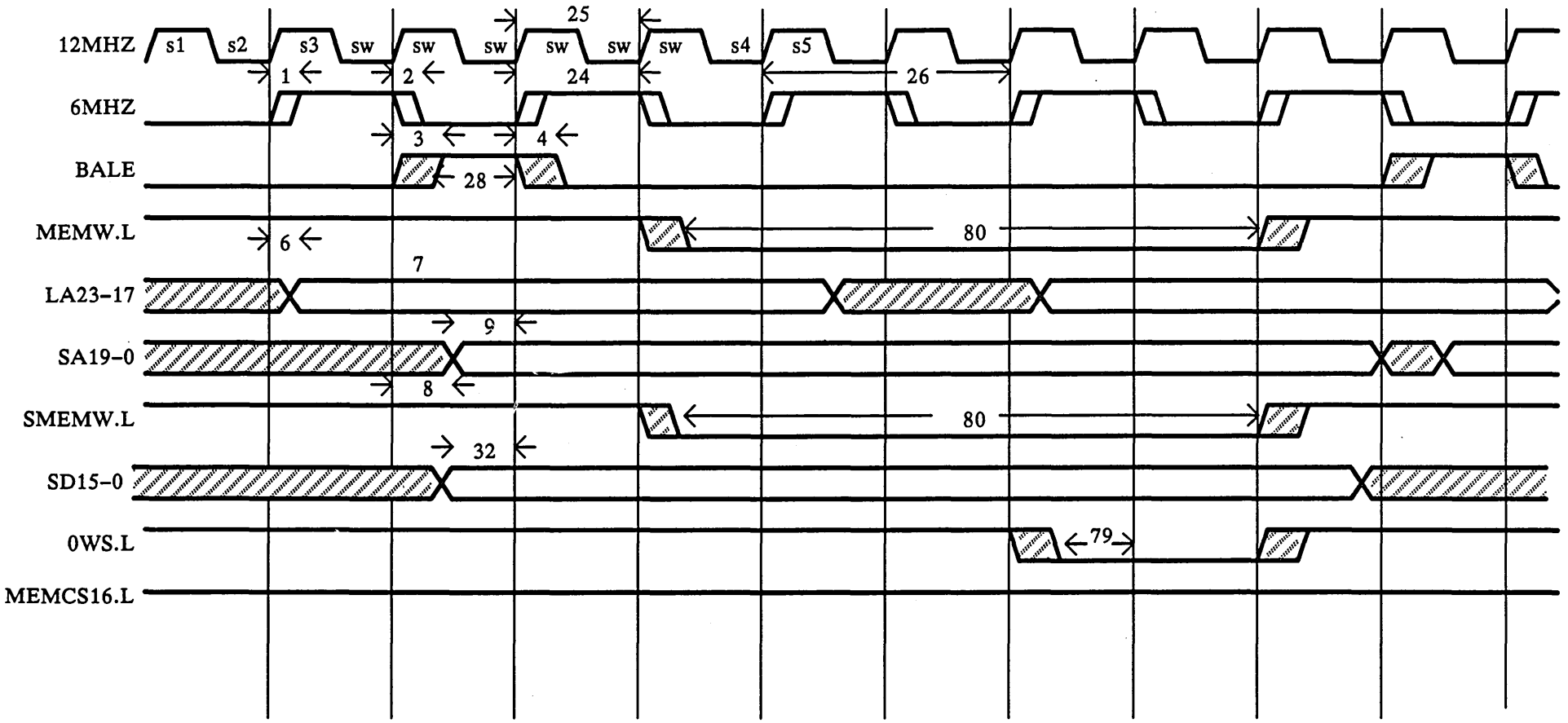


Figure A-13. Bus 8-Bit Memory Write Cycle (Zero Wait State)

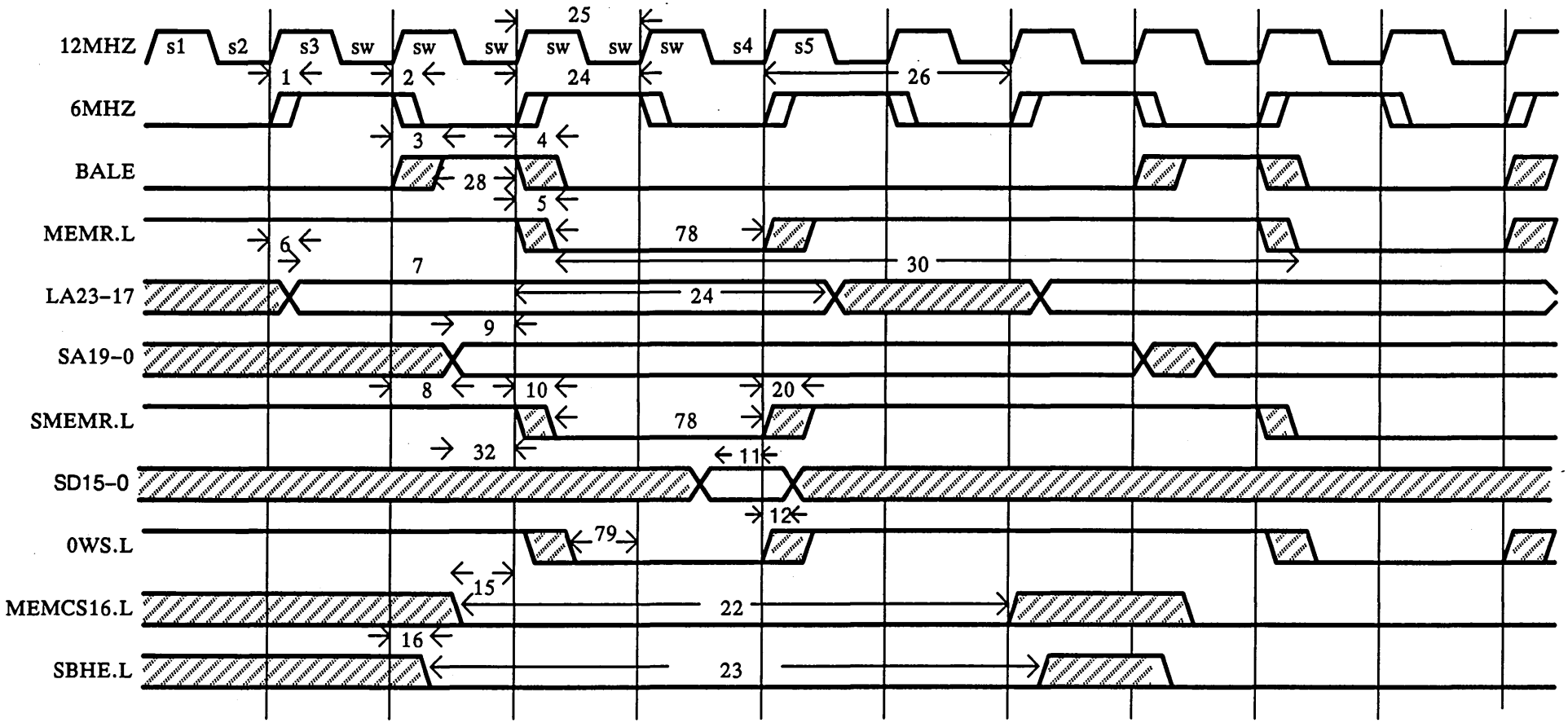


Figure A-14. Bus 16-Bit Memory Read Cycle (Zero Wait State)

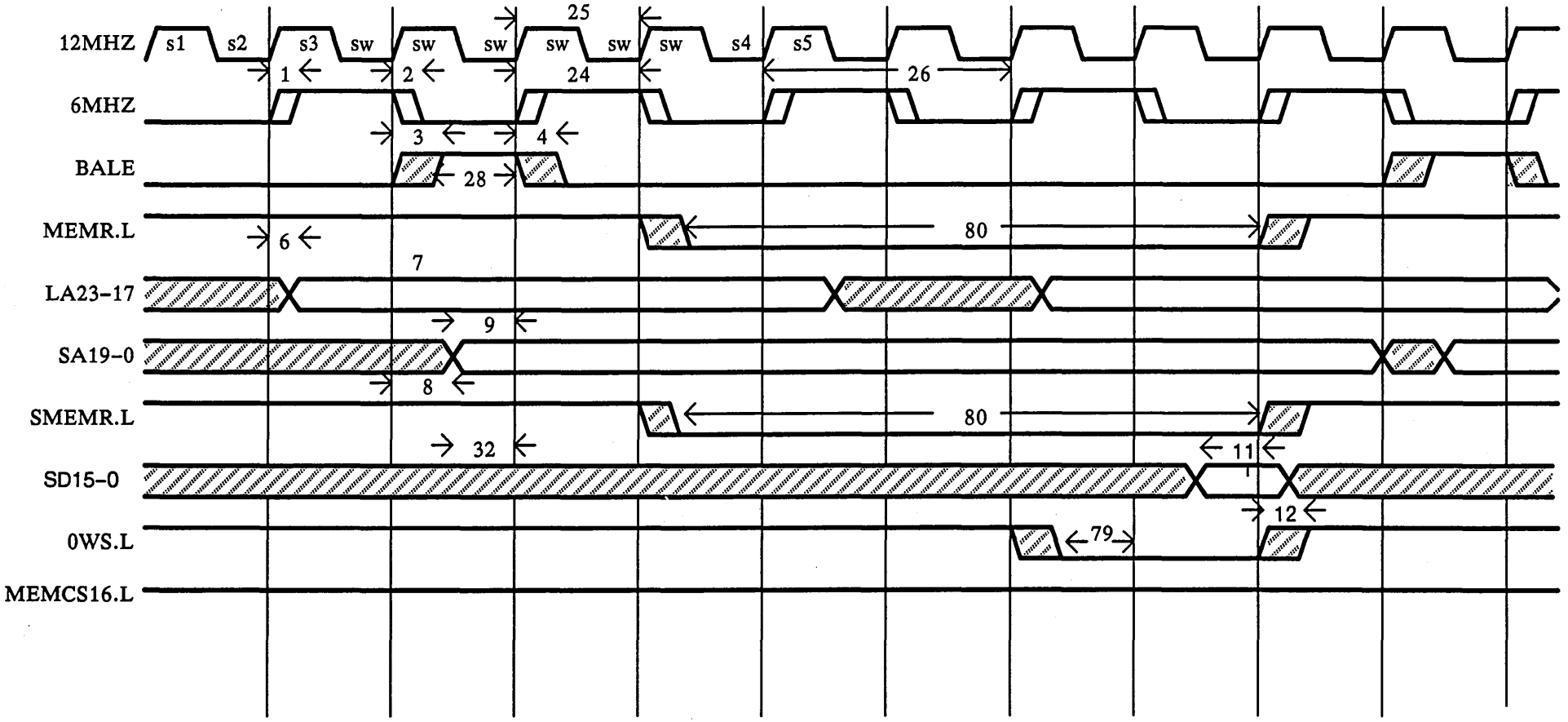


Figure A–15. Bus 8–Bit Memory Read Cycle (Zero Wait State)

Appendix B

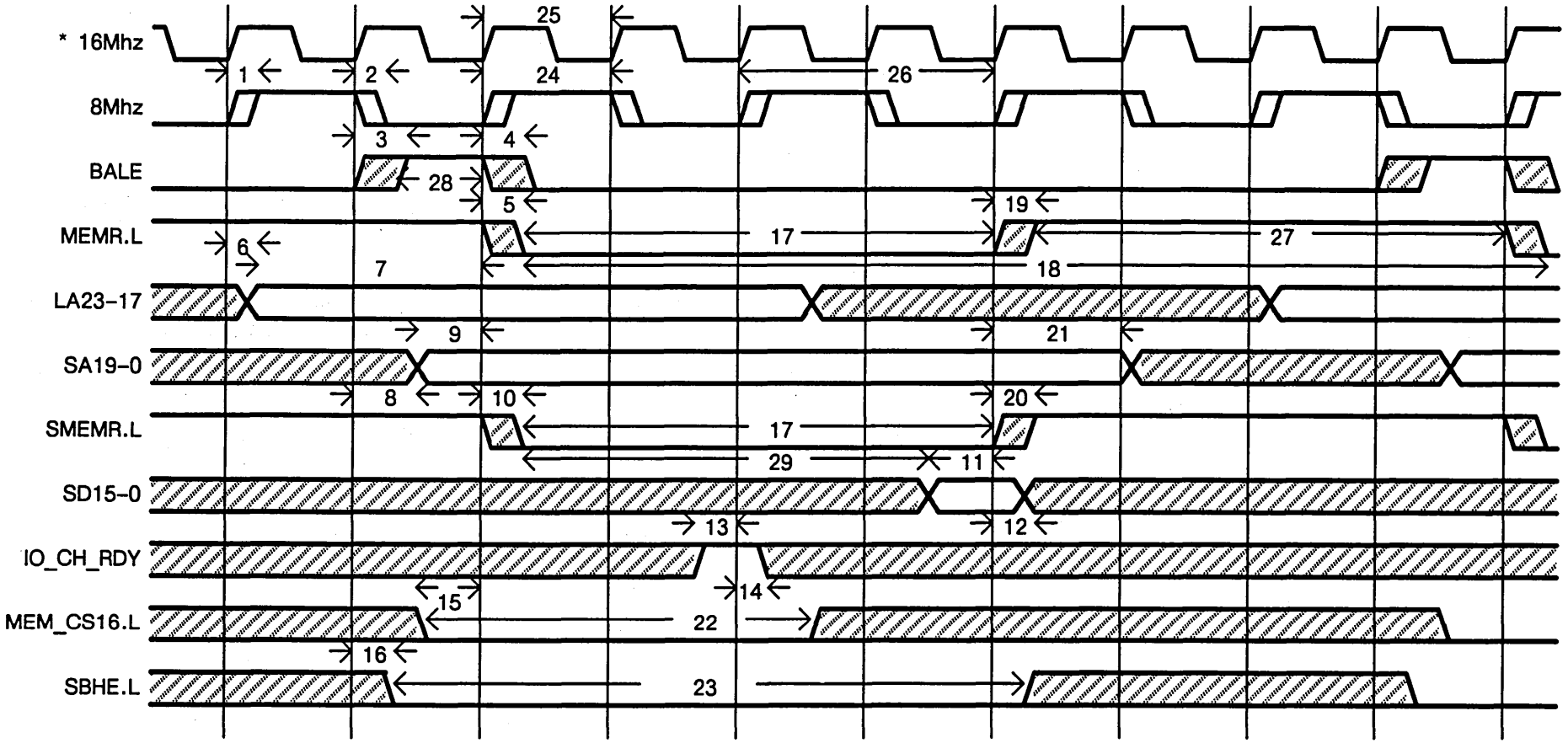
Series 4000 AT-Compatible Bus Timing Diagrams

This appendix contains timing diagrams for the 8-MHz, AT-compatible bus processes in the Series 4000. Table A-1 contains reference information for the cycle times shown in the timing diagrams contained in this chapter. Find the reference number in a diagram and refer to the table for the correct cycle times.

Table B-1. Series 4000 AT-Compatible Bus Cycle Times

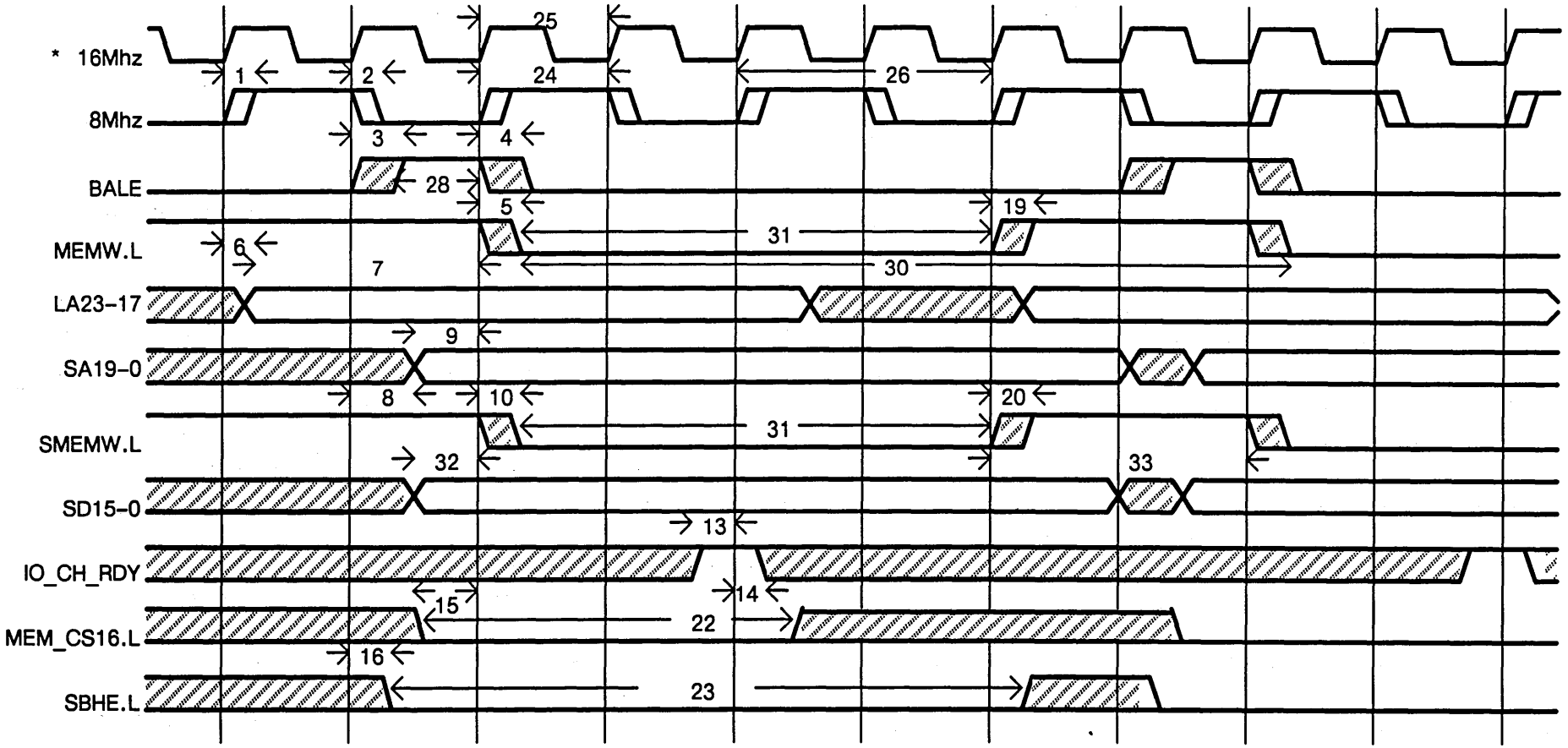
Number	Characteristic	Time (Nanoseconds) Minimum	Maximum
1	CLOCK High to BUS CLOCK High	0	15
2	CLOCK High to BUS CLOCK Low	0	15
3	CLOCK High to BALE High	0	30
4	CLOCK High to BALE Low	0	30
5	CLOCK High to MEMR.L Low	0	22
6	CLOCK High to LA23 - LA17 Valid	0	10
7	LA23 - LA17 Valid to MEMR.L Asserted	115	—
8	CLOCK High to SA19 - SA0 Valid	0	35
9	SA19 - SA0 Valid to MEMR.L Asserted	28	—
10	CLOCK High to SMEMR.L Asserted	0	22
11	SD15 - SD0 Valid to CLOCK High	30	—
12	CLOCK High to SD15 - SD0 Invalid	10	—
13	IO_CH_RDY Asserted to CLOCK High	20	—
14	CLOCK High to IO_CH_RDY Negated	10	—
15	MEM_CS16.L Asserted to CLOCK High	37	—
16	CLOCK High to SBHE.L Asserted	0	22
17	MEMR.L, SMEMR.L Width Asserted	250	—
18	Memory Read Cycle Time	375	—
19	CLOCK High MEMR.L Negated	0	22
20	CLOCK High SMEMR.L Negated	0	22
21	CLOCK High SA19 - SA0 Invalid	62	—
22	MEM_CS16.L Width Asserted	190	—
23	SBHE.L Width Asserted	310	—
24	BUS CLOCK Width High	55	70
25	16Mhz CLOCK Cycle Time	—	62
26	BUS CLOCK Cycle Time	—	125
27	MEMR.L Width High	125	—
28	BALE Width Asserted High	55	70
29	SD15 - SD0 Valid from MEMR.L Asserted	195	—
30	Memory Write Cycle Time	375	—
31	MEMW.L, SMEMW.L Width Asserted	250	—
32	SD15 - SD0 Valid to MEMW.L, SMEMW.L	20	—
33	MEMW.L, SMEMW.L Width negated	125	—
34	SA19 - SA0 Valid to IOW.L Asserted	90	—
35	IO_CS16.L Width Asserted	162	—
36	IO_CS16.L to CLOCK High	37	—
37	IOR.L, IOW.L Width Asserted	185	—
38	SD15 - SD0 Valid from IOR.L, IOW.L High	40	—
39	SA19 - SA0 Valid from IOR.L, IOW.L High	40	—
40	SD15 - SD0 Valid to CLOCK High	30	—
41	CLOCK High to SD15 - SD0 Invalid	10	—
42	BALE to SMEMW.L Asserted	0	30
43	SMEMW.L Width Asserted	560	—
44	SA19 - SA0 Valid to SMEMW.L Asserted	100	—
45	MEM_CS16.L Negated to CLOCK High	37	—
46	SD Valid to SMEMW.L Asserted	90	—
47	SD Valid to IOW.L Asserted	90	—
48	IOR.L, IOW.L Width Asserted	560	—
49	IO_CS16.L Negated to CLOCK High	37	—
50	CLOCK High to IOR.L, IOW.L	0	22
51	CLOCK High to IOR.L, IOW.L Negated	0	22
52	CLOCK High to AEN Asserted	0	60
53	CLOCK High to AEN Negated	0	60
54	MEMR.L Width Asserted	250	—
55	BALE Width Asserted	625	—
56	SA7 - SA0 Valid to MEMR.L Asserted	125	—
57	CLOCK High to REFRESH.L Asserted	0	20
58	CLK Low to DACK High	—	170
59	CLK Low to AEN High	—	200
60	Address Float to Active from CLK High	—	170
61	READ or WRITE Active from CLK High	—	150
62	CLK High to READ or WRITE High	—	190
63	CLK High to WRITE High	—	130
64	CLK High to READ High	—	190
65	CLK High to TC High	—	170
66	CLK High to TC Low	—	170
67	DRQ to CLK Low Setup Time	0	—
68	CLK Low to DACK Low	—	170
69	CLK High to AEN Low	—	130
70	WRITE High to Address Hold Time	—	283
71	CLK High to READ or WRITE Float	—	120
72	MASTER.L Negated from DRQ Negated	—	250
73	SA19-0, LA23-17 Tristate Master Negated	—	50
74	DACK Asserted to MASTER.L Asserted	50	—
75	Bus Driven from MASTER Asserted	125	—
76	MEMCMD, IOCMD Asserted from Master.L	250	—
77	Master Width Asserted	—	12 µs
78	MEMR.L, SMEMR.L, 0WS Width Asserted	125	—
79	0WS to CLK High	30	—
80	MEMR/W, SMEMR/W, OWS	313	—
81	MEMR.L to valid SD15-0	—	250
82	MEMR.L to SD15-0 invalid	—	80
83	IOR.L to SD15-0 valid	—	200
84	IOR.L to SD15-0 invalid	—	0

VCC = 4.75 V dc to 5.25 V dc TA = 0°to 70°C



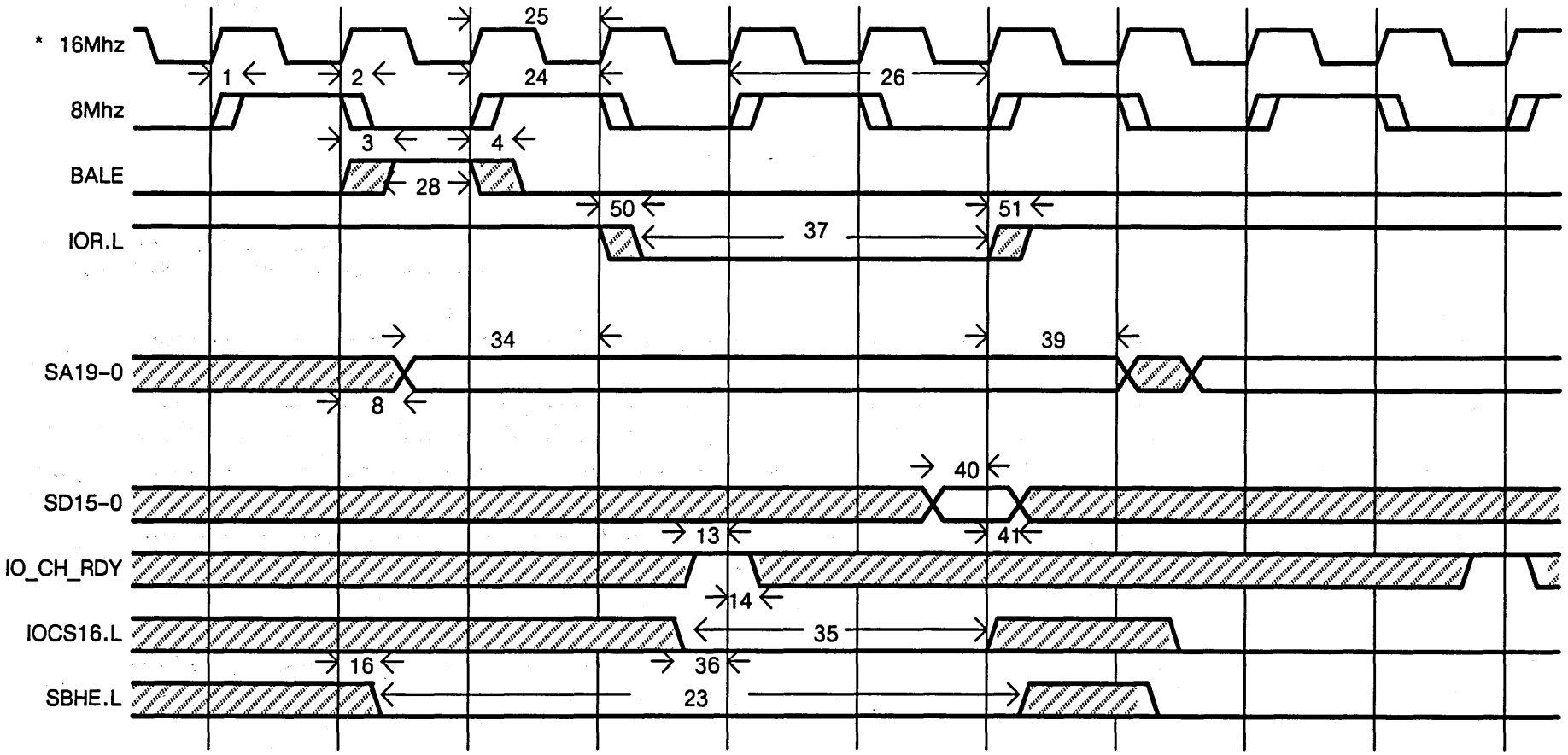
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-1. Bus 16-Bit Memory Read Cycle



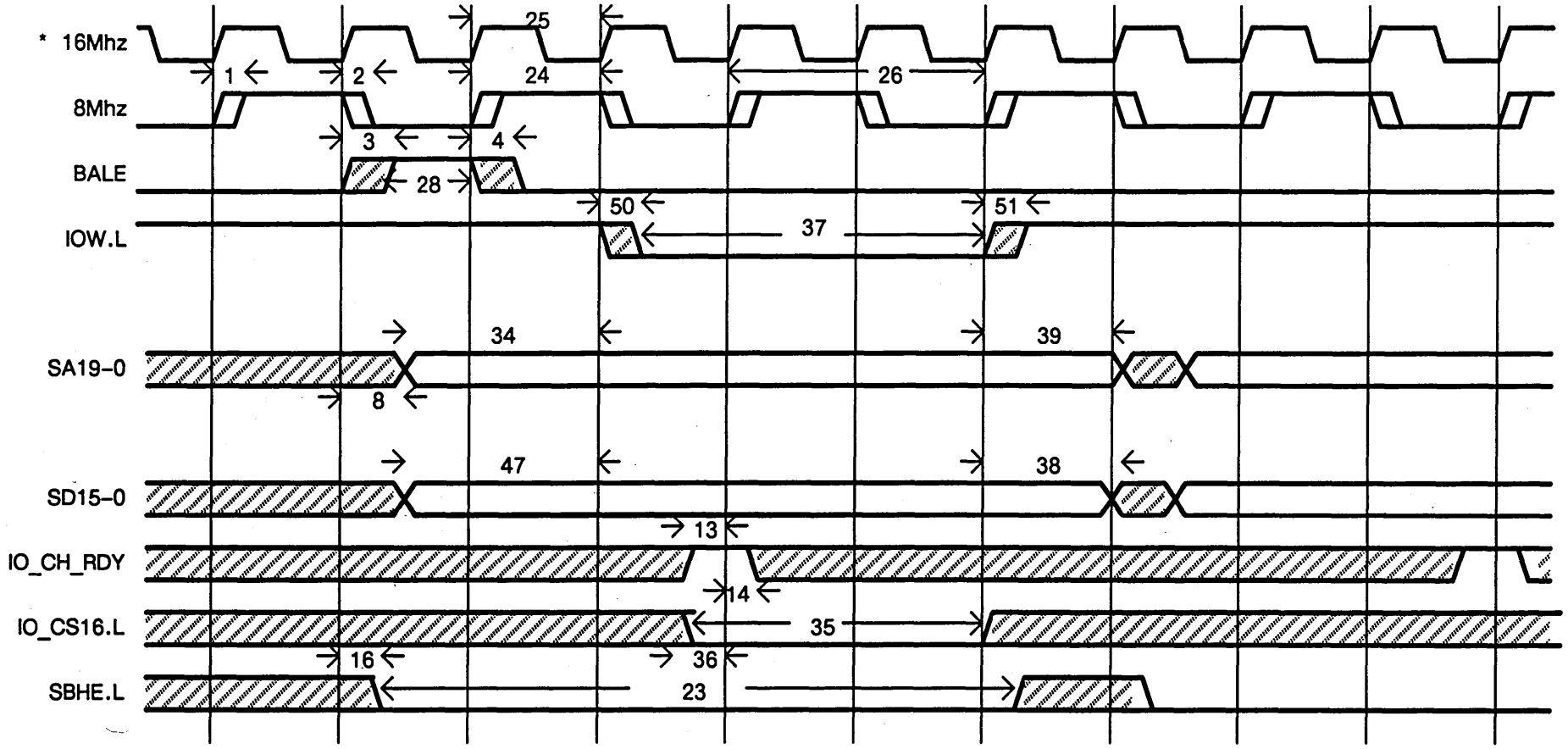
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-2. Bus 16-Bit Memory Write Cycle



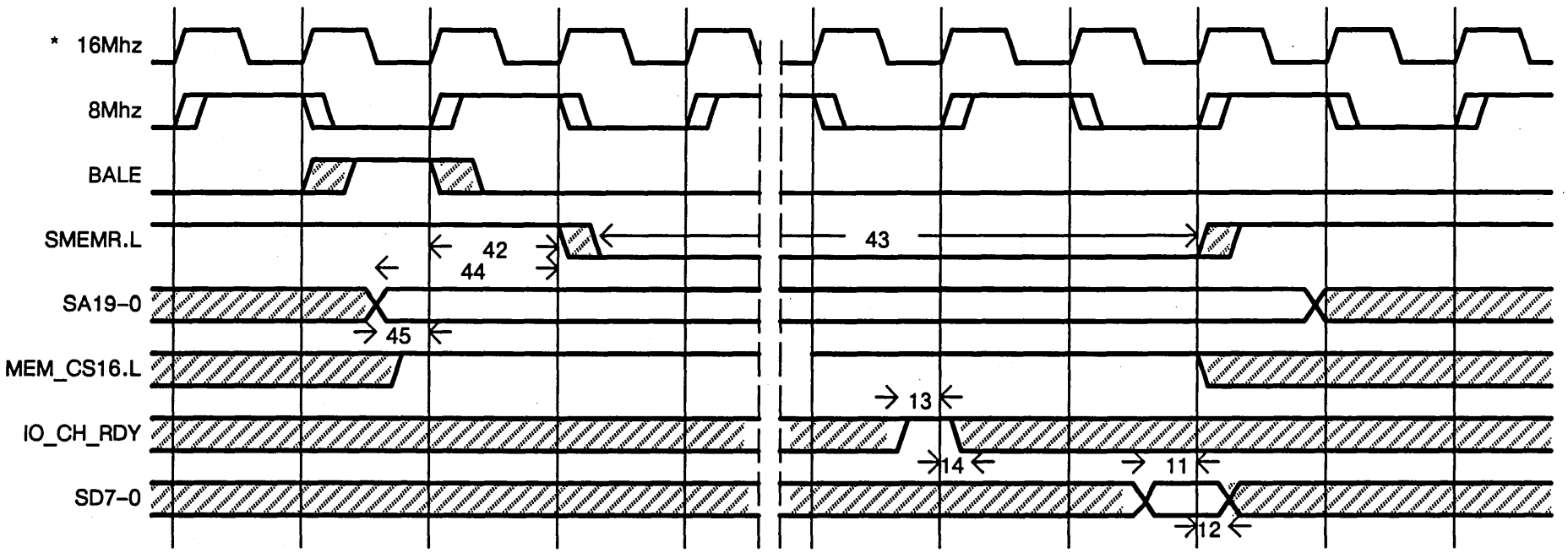
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B–3. Bus 16–Bit I/O Read Cycle



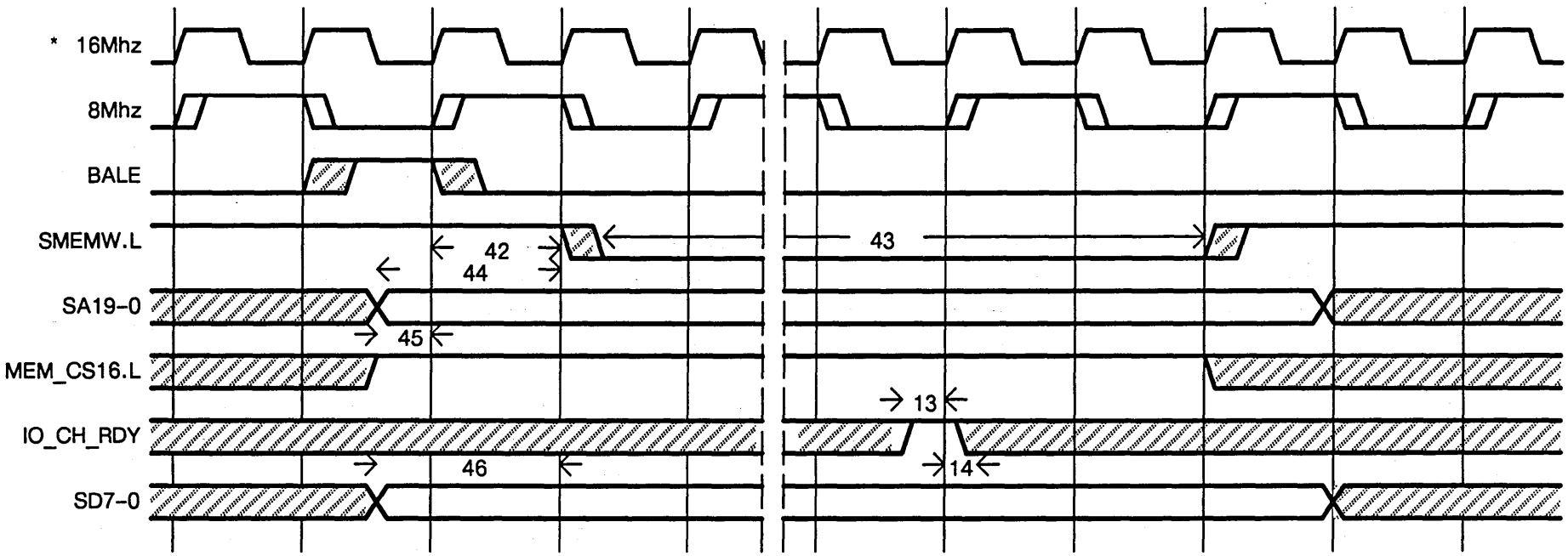
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B–4. Bus 16-Bit I/O Write Cycle



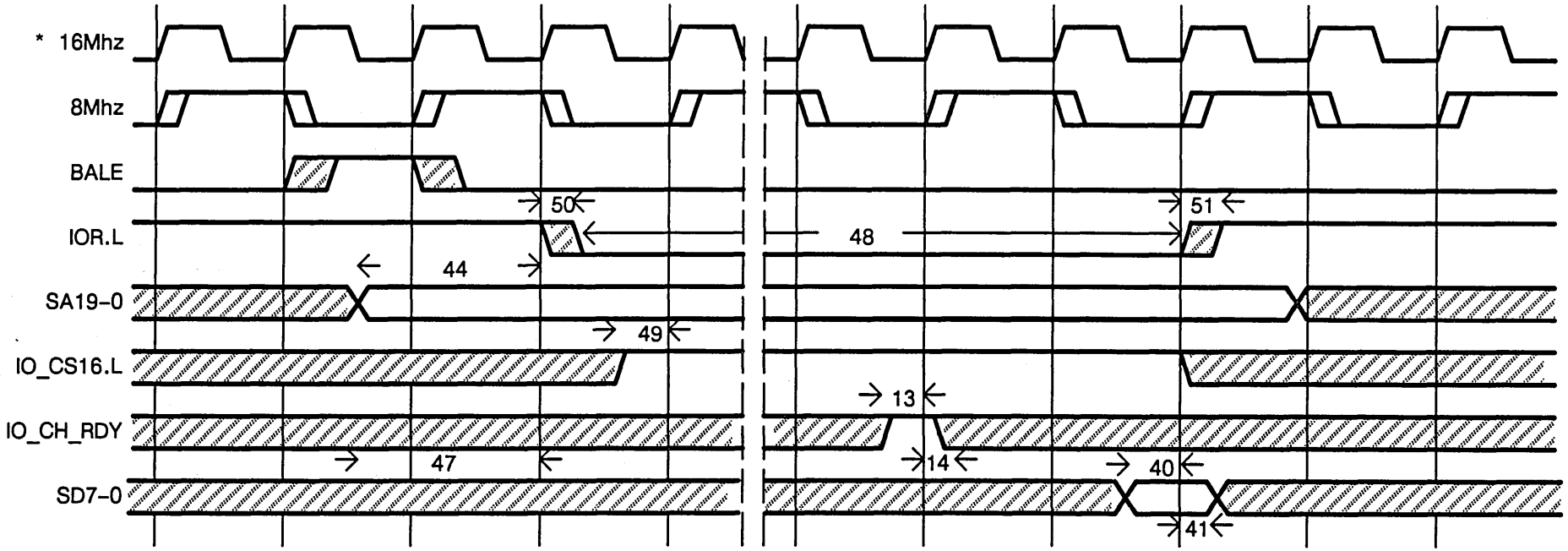
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-5. Bus 8-Bit Memory Read Cycle



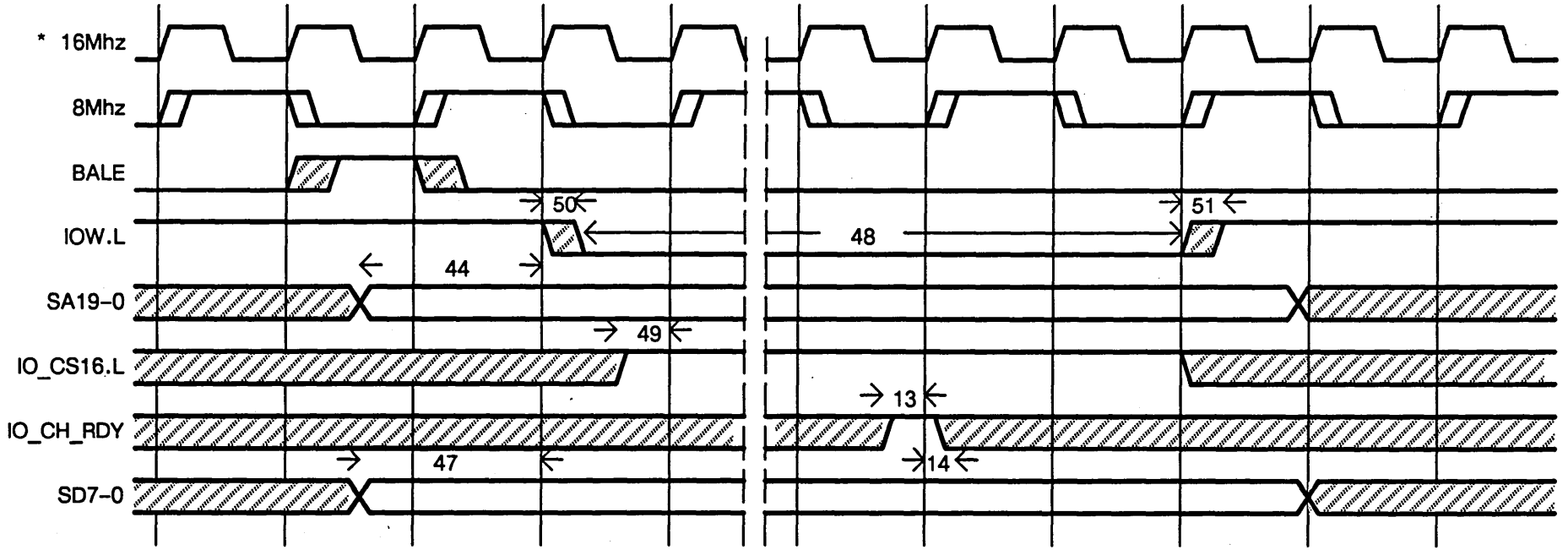
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-6. Bus 8-Bit Memory Write Cycle



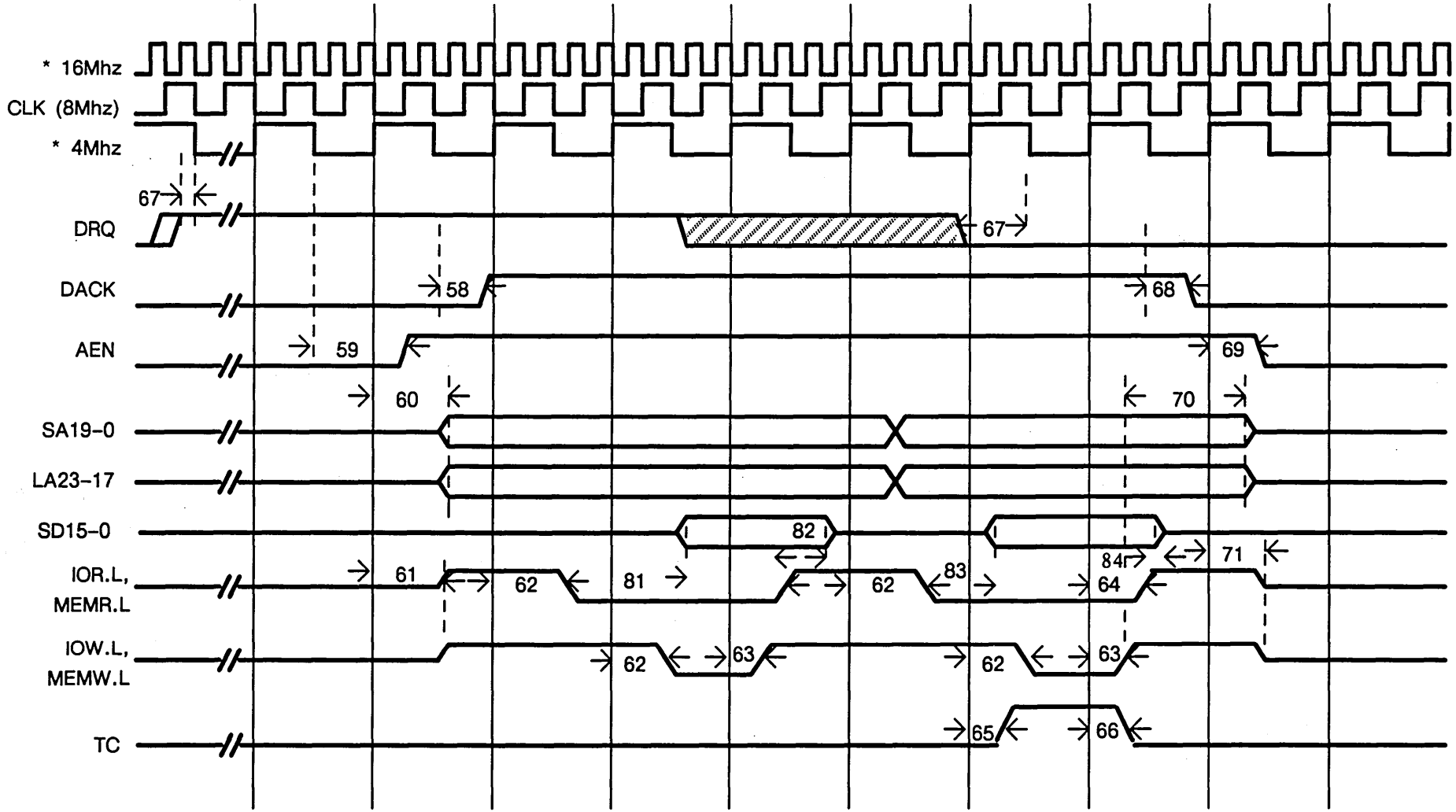
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-7. Bus 8-Bit I/O Read Cycle



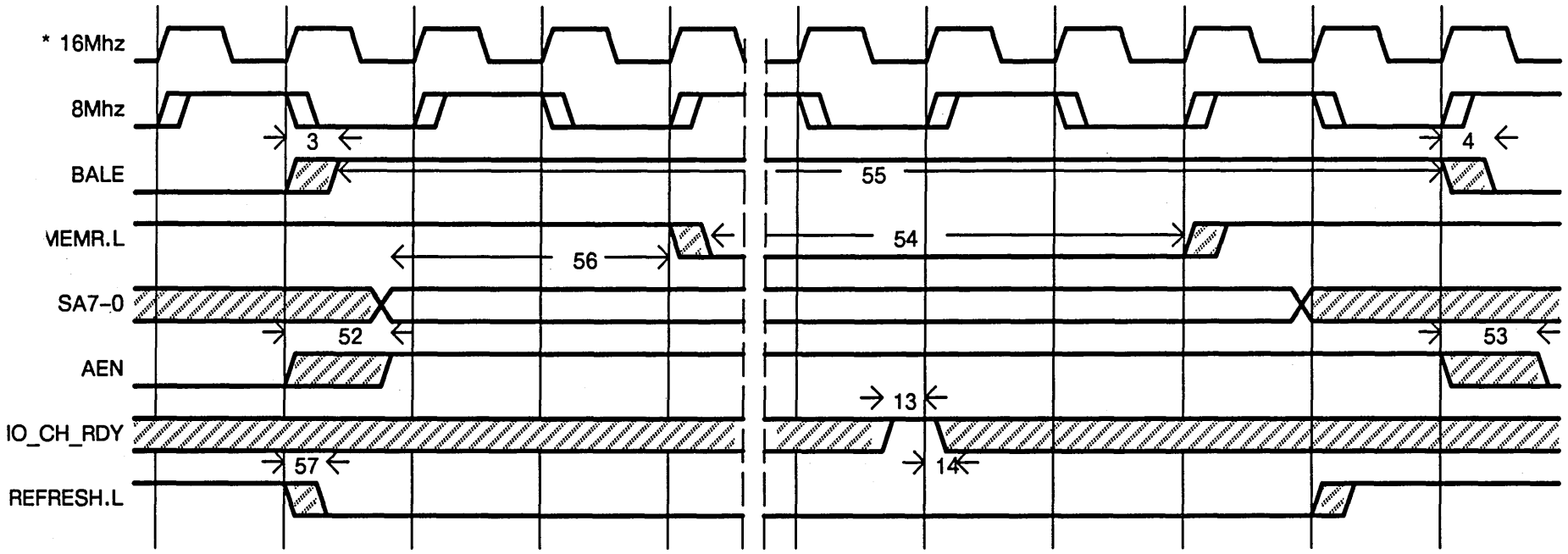
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-8. Bus 8-Bit I/O Write Cycle



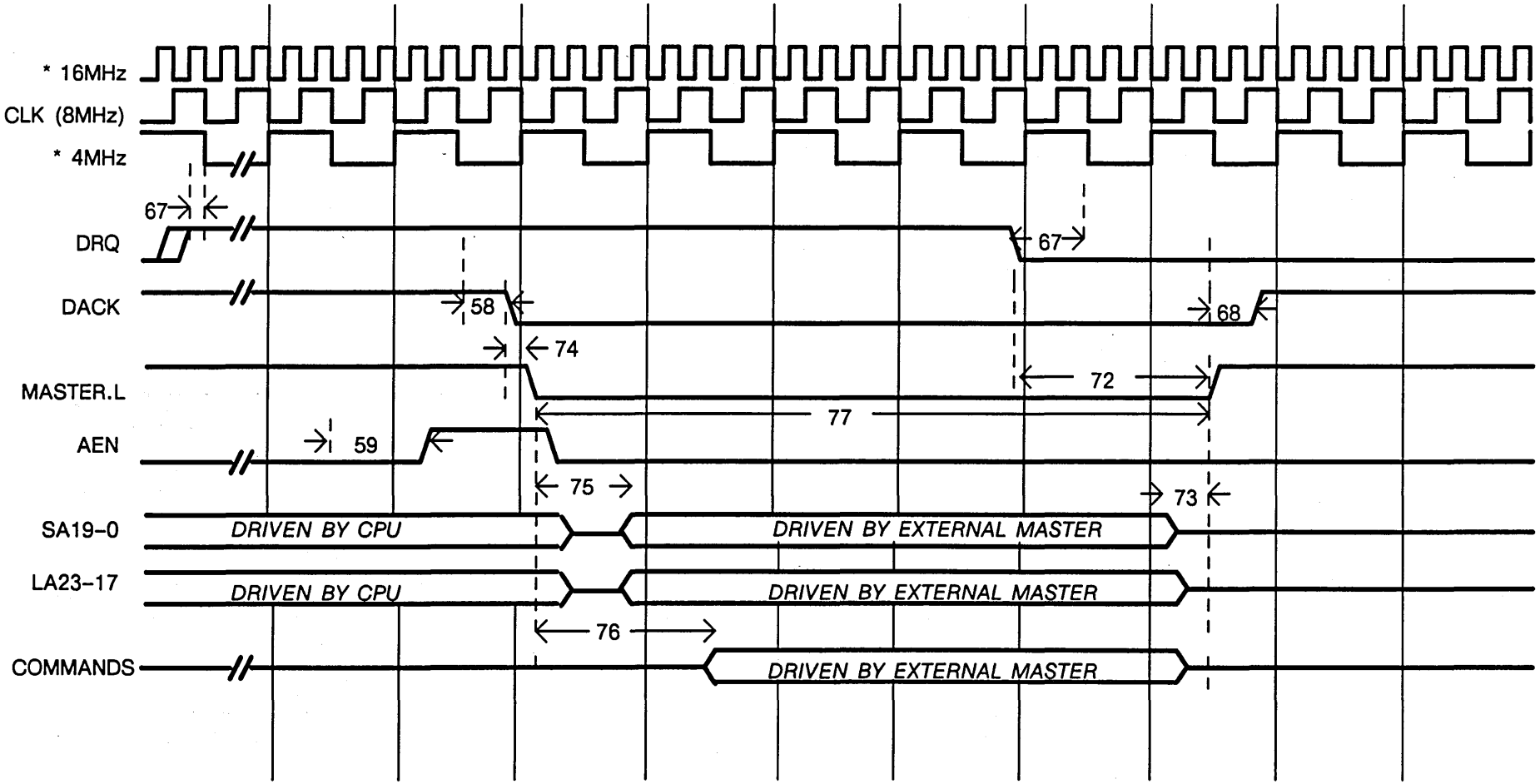
* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B-9. Bus DMA Cycles



* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B–10. Bus Refresh Cycle



* Internal signal on the CPU/Motherboard.
Not available on the Bus.

Figure B–11. External Mastership

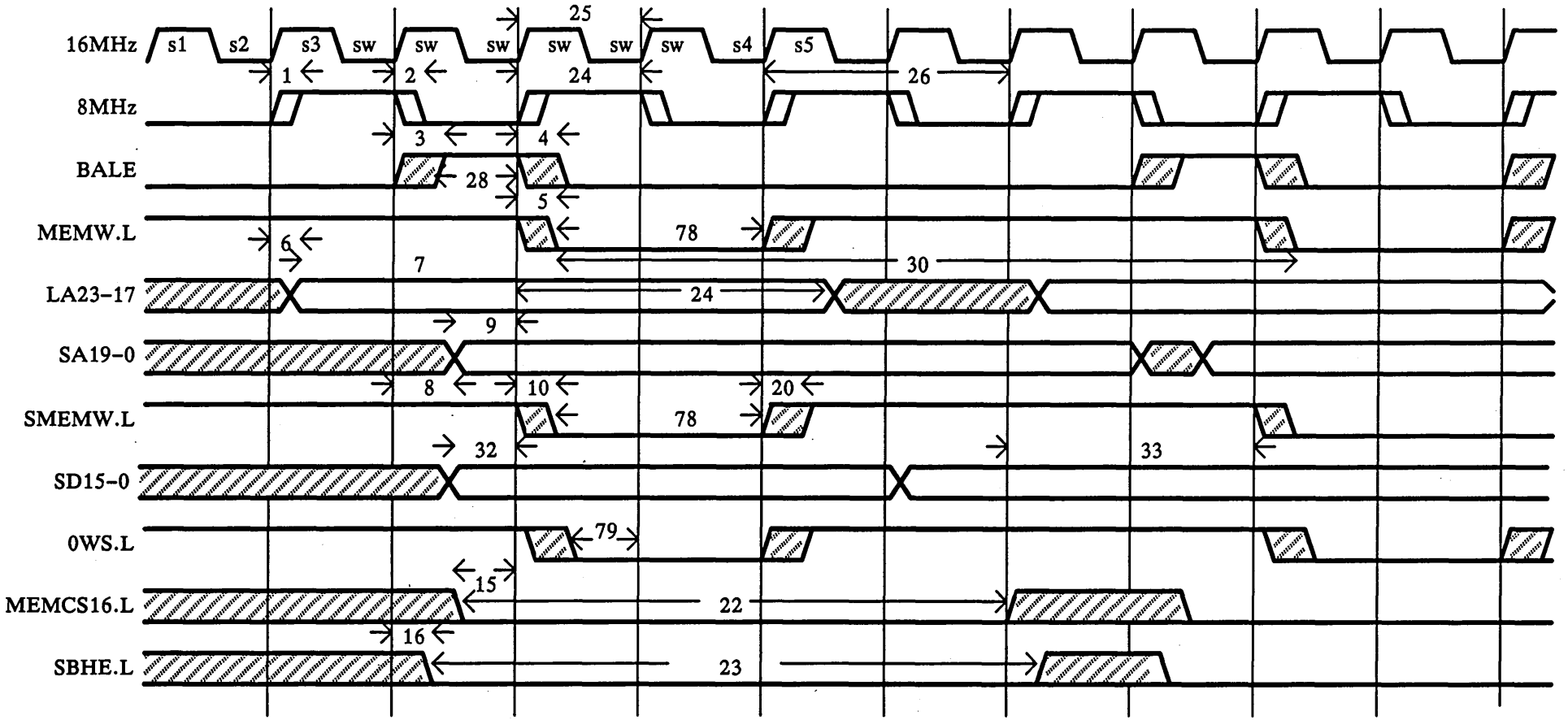


Figure B–12. Bus 16–Bit Memory Write Cycle (Zero Wait State)

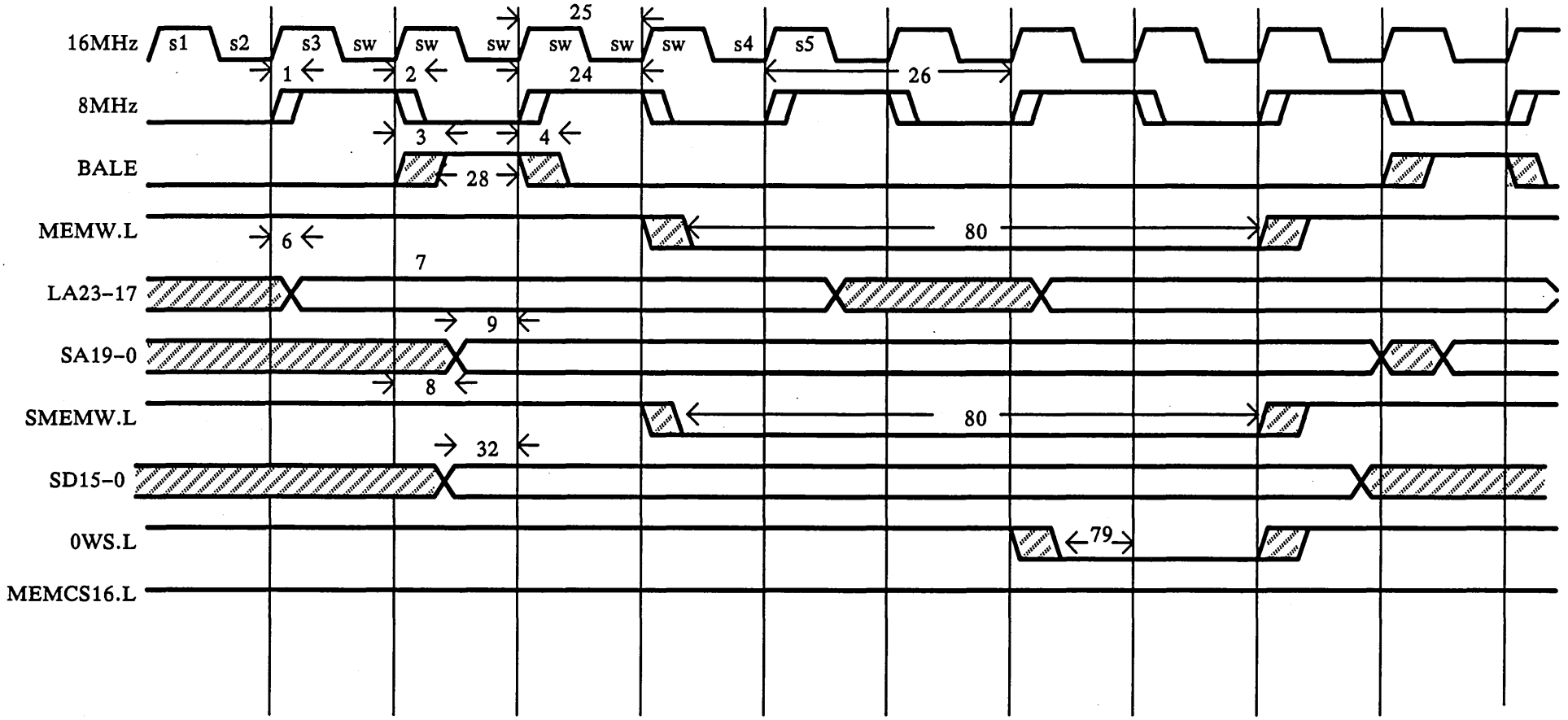


Figure B-13. Bus 8-Bit Memory Write Cycle (Zero Wait State)

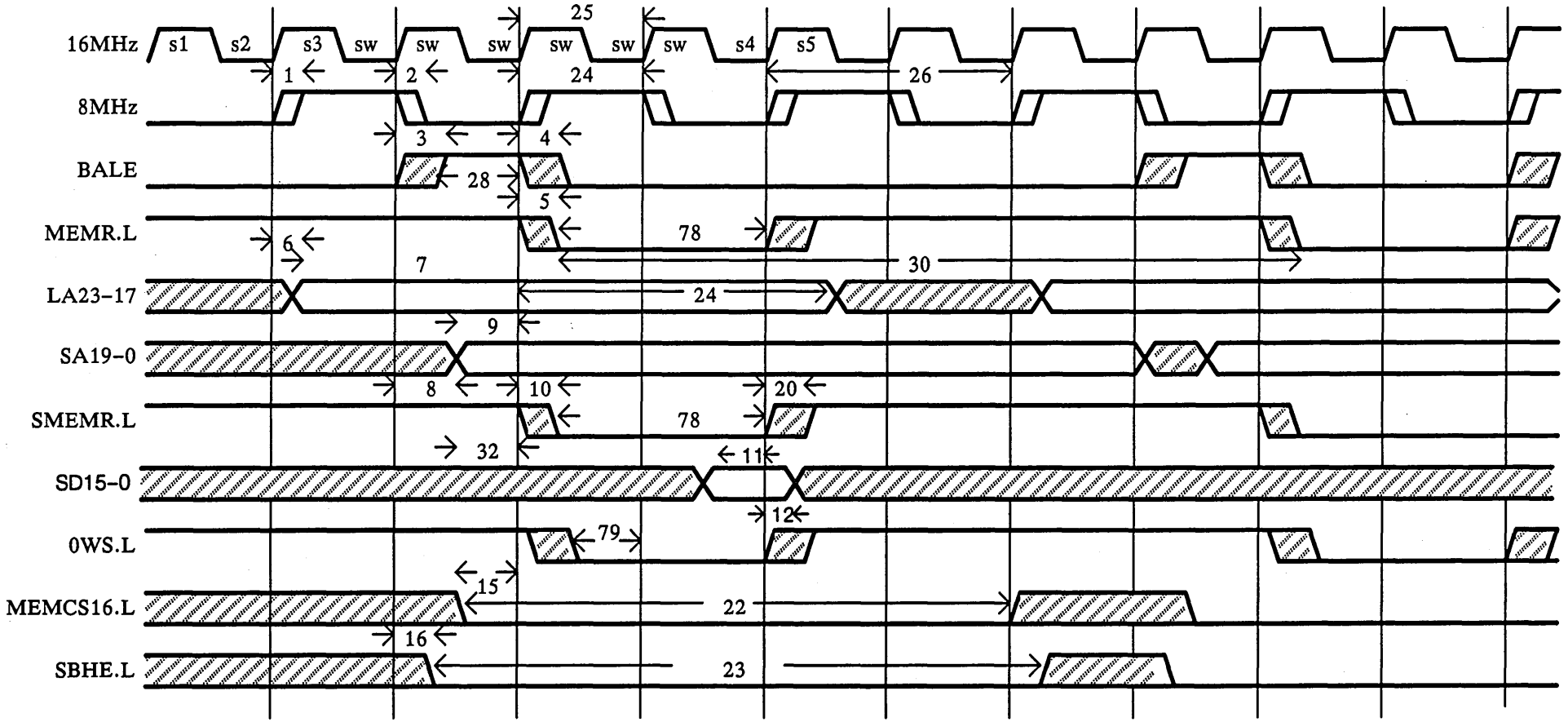


Figure B-14. Bus 16-Bit Memory Read Cycle (Zero Wait State)

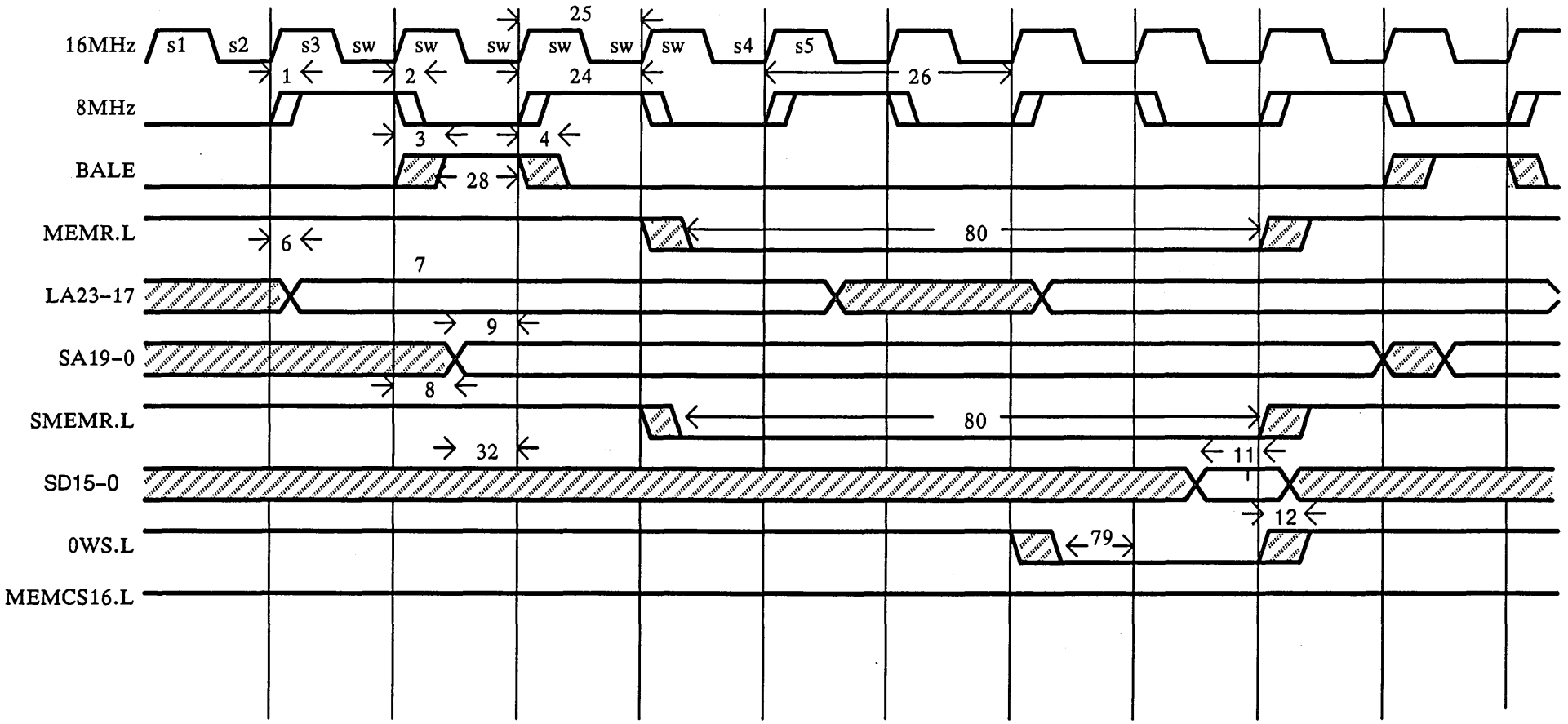


Figure B-15. Bus 8-Bit Memory Read Cycle (Zero Wait State)

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